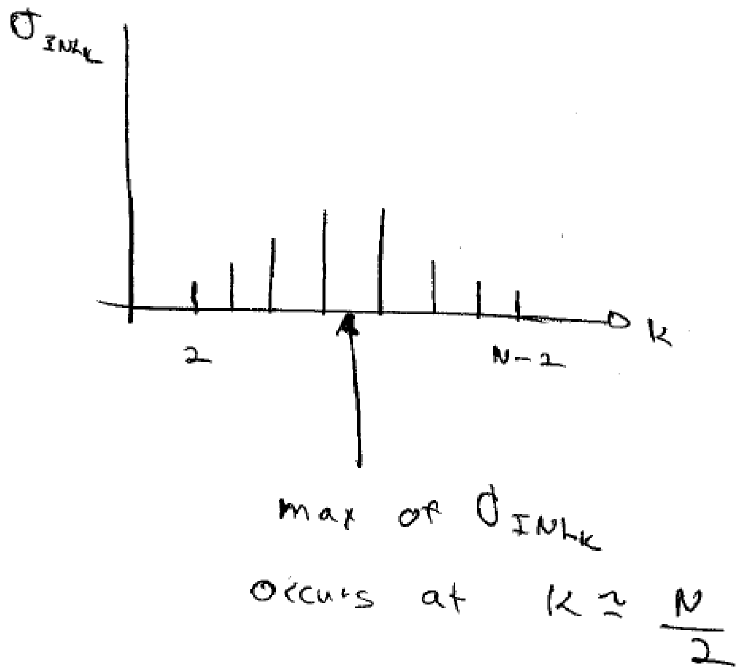
EE 505

Lecture 11

- Formalization of Statistical Models
- Offset Voltages

String DAC Statistical Performance

INL_k assumes a maximum variance at mid-code

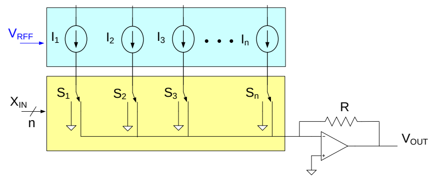


$$\sigma_{INLk\,\max} = \sigma_{\frac{R_R}{R_{NOM}}} \frac{\sqrt{N}}{2}$$

Review from Last Lecture

Current Steering DAC Statistical Characterization

Binary Weighted



$$\sigma_{INL_{b=<1000..0>}} = \sqrt{\frac{N}{2}\left[1-\frac{N/2}{N-1}\right]^2 + \left(\frac{N}{2}-1\right)\left[\frac{N/2}{N-1}\right]^2} \bullet \sigma_{\frac{I_{RGk}}{I_{LSBX}}}$$

$$\sigma_{INL_{MAX}} \cong \sigma_{INL_{b=<1,0,...0>}} \cong \frac{\sqrt{N}}{2}\sigma^2_{\frac{I_{RG}}{I_{LSBX}}}$$

Note this is the same result as obtained for the unary DAC

But closed form expressions do not exist for the INL of this DAC since the INL is an order statistic

Review from Last Lecture

Statistical Modeling of Current Sources

$$\sigma_{\frac{I_{DR}}{I_{DN}}} = \sqrt{\sigma^2_{\frac{\mu_R}{\mu_N}} + \sigma^2_{\frac{C_{OXR}}{C_{OXN}}} + 4\left(\frac{V_{THN}}{V_{GS}-V_{THN}}\right)^2 \sigma^2_{\frac{V_{THR}}{V_{THN}}}}$$

or

$$\sigma_{\frac{I_{DR}}{I_{DN}}} = \sqrt{\sigma^2_{\frac{\mu_R}{\mu_N}} + \sigma^2_{\frac{C_{OXR}}{C_{OXN}}} + \left(\frac{2}{V_{GS}-V_{THN}}\right)^2 \sigma^2_{V_{THR}}}$$

It will be assumed that
(will discuss assumption later)

$$\sigma^2_{\frac{\mu_R}{\mu_N}} = \frac{A_\mu^2}{WL}$$

$$\sigma^2_{\frac{C_{OXR}}{C_{OXN}}} = \frac{A_{Cox}^2}{WL}$$

$$\sigma^2_{V_{THR}} = \frac{A_{VT0}^2}{WL}$$

where A_μ,A_{Cox},A_{VT0} are Pelgrom process parameters

$$\sigma_{\frac{I_{DR}}{I_{DN}}} = \frac{1}{\sqrt{WL}}\sqrt{A_\mu^2 + A_{Cox}^2 + \frac{4}{V_{EB}^2}A_{VT0}^2}$$

Define

$$A_\beta = \sqrt{A_\mu^2 + A_{Cox}^2}$$

Thus

$$\sigma_{\frac{I_{DR}}{I_{DN}}} = \frac{1}{\sqrt{WL}}\sqrt{A_\beta^2 + \frac{4}{V_{EB}^2}A_{VT0}^2}$$

Often only A_β is available

Review from Last Lecture

Statistical Modeling of Current Sources

$$\sigma_{\frac{I_{DR}}{I_{DN}}} = \frac{1}{\sqrt{WL}}\sqrt{A_{\beta}^{2} + \frac{4}{V_{EB}^{2}}A_{VT0}^{2}}$$

Gate area: A=WL

- Standard deviation decreases with $\sqrt{A}$
- Large V_{EB} reduces standard deviation
- Operating near cutoff results in large mismatch
- Often threshold voltage variations dominate mismatch

$$\sigma_{\frac{I_{DR}}{I_{DN}}} \cong \frac{2}{V_{EB}\sqrt{WL}}A_{VT0}$$

Theorem: If the random part of two uncorrelated current sources I_1 and I_2 are identically distributed with normalized variance, $\sigma^2_{I_R/I_N}$ then the random variable $\Delta I = I_2 - I_1$ has a variance given by the equation $\sigma^2_{\Delta I/I_N} = 2\sigma^2_{I_R/I_N}$

Proof:

$$\Delta I = I_1 - I_2$$

$$\frac{\Delta I}{I_N} = \frac{I_1}{I_N} - \frac{I_2}{I_N}$$

$$\frac{\Delta I}{I_N} = \frac{I_N + I_{R1}}{I_N} - \frac{I_N + I_{R2}}{I_N} = \frac{I_{R1}}{I_N} - \frac{I_{R2}}{I_N}$$

$$\sigma^2_{\frac{\Delta I}{I_N}} = \sigma^2_{\frac{I_R}{I_N}} + \sigma^2_{\frac{I_R}{I_N}} = 2\sigma^2_{\frac{I_R}{I_N}} \qquad \blacksquare$$

Statistical Modeling of Circuits

The previous statistical analysis was somewhat tedious

Will try to formalize the process for obtaining two important statistics, the mean and variance, of a function of interest

Assume Y is a function of n uncorrelated random variables $x_{R1},\ldots x_{Rn}$ where the mean and variance of x_{Ri} are "small"

$$Y = f\left(x_{R1}, x_{R2}, \ldots x_{Rn}\right)$$

$$X_R = \begin{bmatrix} x_{R1} \\ x_{R2} \\ \ldots \\ x_{Rn} \end{bmatrix}$$

pdf of the random part of Y is invariably highly nonlinear joint function of a large number of random variables

Recall if $\left(x_{R1}, x_{R2}, \ldots x_{Rn}\right)$ uncorrelated and $f = \sum_{i=1}^{m} a_i x_{Ri}$ then $\sigma_f^2 = \sum_{i=1}^{m} a_i^2 \sigma_{x_{Ri}}^2$

Since random variables are invariably small, will try to linearize the dependence of the random variables on Y and use previous theorem to obtain μ and σ

Statistical Modeling of Circuits

$$Y = f\left(x_{R1}, x_{R2}, \ldots x_{Rn}\right) \qquad X_R = \begin{bmatrix} x_{R1} \\ x_{R2} \\ \ldots \\ x_{Rn} \end{bmatrix}$$

Assuming means are all 0, Y can be expressed in a Taylor's series expanded around mean as

$$Y = f\left(X\right)\Big|_{X_R=0} + \sum_{j=1}^{n} \frac{\partial f}{\partial x_{Rj}}\Bigg|_{X_R=0} x_{Rj} + \varepsilon\left(x_{R1}, x_{R2}, \ldots x_{Rn}\right)$$

where $\varepsilon\left(x_{R1}, x_{R2}, \ldots x_{Rn}\right)$ is due to higher-order terms and is small

Statistical Modeling of Circuits

$$Y \simeq f(X)\Big|_{X_R=0} + \sum_{j=1}^{n} \frac{\partial f}{\partial x_{Rj}}\Bigg|_{X_R=0} x_{Rj}$$

Note power series expansion linearized Y in the variables $\left(x_{R1}, x_{R2}, \ldots x_{Rn}\right)$

$$\frac{Y}{Y_N} = \frac{f(X)\Big|_{X_R=0}}{Y_N} + \sum_{j=1}^{n} \frac{1}{Y_N} \frac{\partial f}{\partial x_{Rj}}\Bigg|_{X_R=0} x_{Rj}$$

From Theorem:

$$\sigma^2_{\frac{Y}{Y_N}} = \sum_{j=1}^{n} \left(\left(\frac{1}{Y_N} \frac{\partial f}{\partial x_{Rj}}\Bigg|_{X_R=0} \right)^2 \sigma^2_{x_{Rj}} \right)$$

Define:

$$\hat{S}^{f}_{xRj} = \frac{1}{Y_N} \frac{\partial f}{\partial x_{Rj}}\Bigg|_{X_R=0}$$

$$\sigma^2_{\frac{Y}{Y_N}} = \sum_{j=1}^{n} \left(\left[\hat{S}^{f}_{xRj} \right]^2 \sigma^2_{x_{Rj}} \right)$$

Statistical Modeling of Circuits

But

$$\sigma^2_{\frac{Y}{Y_N}} = \sum_{j=1}^{n} \left(\left[\hat{S}^{f}_{xRj} \right]^2 \sigma^2_{x_{Rj}} \right) = \sum_{j=1}^{n} \left(\left[\hat{S}^{f}_{xRj} \right]^2 \left(\frac{x_{jN}}{x_{jN}} \right)^2 \sigma^2_{x_{Rj}} \right) = \sum_{j=1}^{n} \left(\left[x_{jN} \hat{S}^{f}_{xRj} \right]^2 \sigma^2_{\frac{x_{Rj}}{x_{jN}}} \right)$$

Alternatively, from the more standard definition of sensitivity $S^{f}_{xR_j}$:

$$S^{f}_{xR_j} = \frac{x_{jN}}{Y_N} \left. \frac{\partial f}{\partial x_{Rj}} \right|_{X_R=0} \quad \Rightarrow \quad S^{f}_{xR_j} = x_{jN} \hat{S}^{f}_{xR_j}$$

we thus obtain

$$\boxed{\sigma^2_{\frac{Y}{Y_N}} = \sum_{j=1}^{n} \left(\left[S^{f}_{xRj} \right]^2 \sigma^2_{\frac{x_{Rj}}{x_{Ni}}} \right)}$$

Statistical Modeling of Circuits

$$\mathrm{Y} = \mathrm{f}\left(x_{R1}, x_{R2}, \ldots x_{Rn}\right)$$

Y is any function of interest

$$\left(x_{R1}, x_{R2}, \ldots x_{Rn}\right)$$ Random part of process parameters

$$\sigma^2_{\frac{\mathrm{Y}}{\mathrm{Y_N}}} = \sum_{j=1}^{n} \left(\left[S^{f}_{xRj} \right]^2 \sigma^2_{\frac{x_{Rj}}{x_{Nj}}} \right)$$

Determined by Circuit

Determined by Process

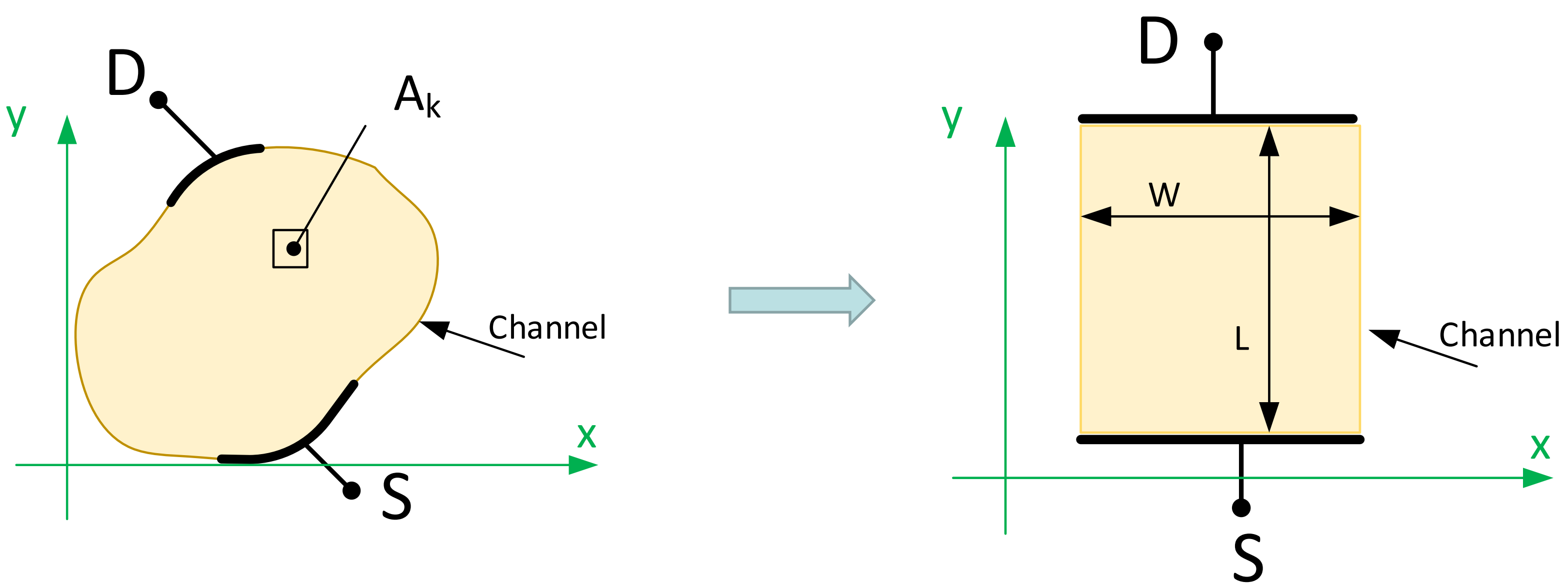
- Determine sensitivity function by analyzing circuit
- Determine variances by characterizing process

This approach is a formalized approach to statistical analysis that is more systematic than the ad hoc approach used in last lecture

Will now focus on characterizing the process parameters

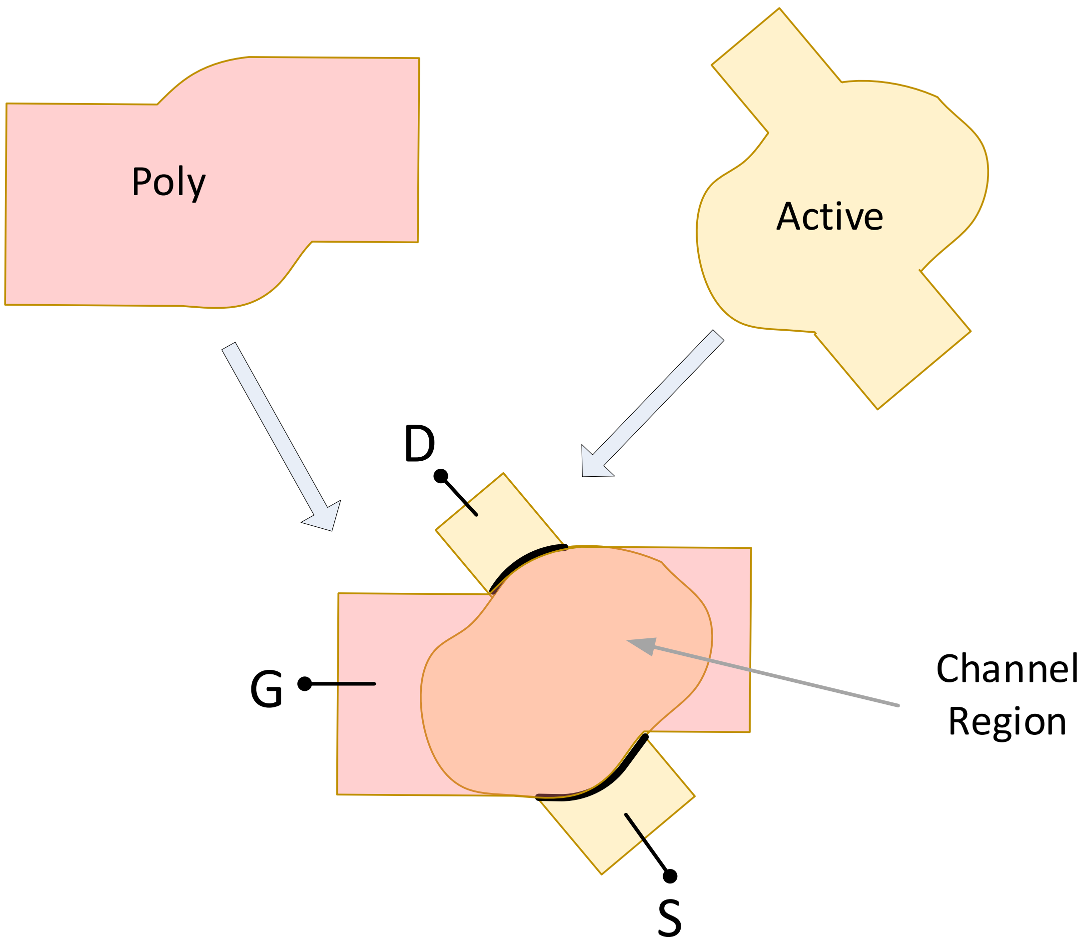
Theorem:

For any arbitrarily shaped transistor there exists a rectangular transistor that has the same static I-V characteristics



Only channel is shown which is the intersection of Poly and Active

Arbitrarily Shaped Transistor



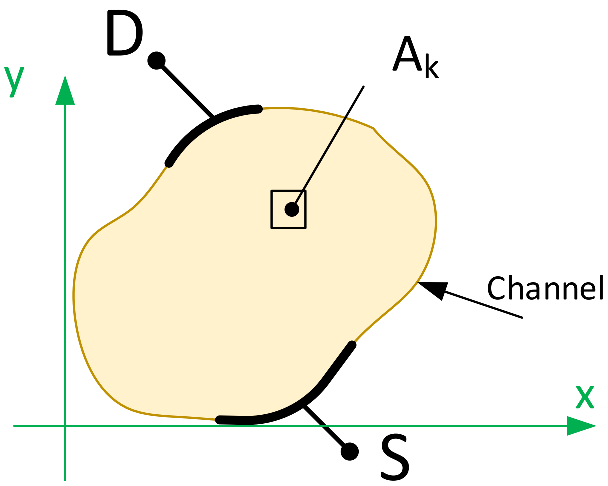
Consider first the mobility

Claim:

$$\sigma^2_{\frac{\mu_R}{\mu_N}} = \frac{A^2_{\mu}}{A}$$

where A_μ is the Pelgrom matching parameter and A is the gate area

Argument:



Assume (define)

$$\mu_{eq} = \frac{\int_A \mu(x,y)\,dxdy}{A}$$

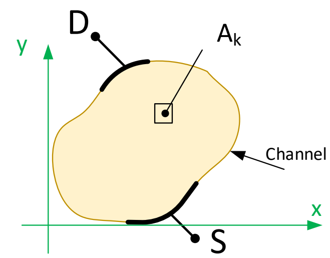
Let S_k be a square of area A_k in the channel

$$\mu_{eq} = \frac{\sum_{i=1}^{N} \int_{A_{ki}} \mu(x,y)\,dxdy}{A}$$

where the channel has been partitioned into N disjoint regions each of area A_{ki}

For convenience, assume $A_{ki}=A_{kj}=A_k$ for all i,j

Claim: $\sigma^2_{\frac{\mu_R}{\mu_N}} = \frac{A_\mu^2}{A}$



Argument continued:

$$\mu_{eq} \simeq \frac{\sum_{i=1}^{N} \int_{A_{ki}} \mu(x,y)\,dxdy}{A}$$

Assume the random variables $\int_{A_{ki}} \mu(x,y)\,dxdy$ are uncorrelated and identically distributed with variance $\sigma^2_{\mu\_A_k}$

It thus follows that $\sigma^2_{\mu_{eq}} \simeq \frac{1}{A^2} N \sigma^2_{\mu\_A_k}$

But nominal A_k is $A_{kN} = A/N$ ⇒ $N = A/A_{kN}$ ⇒ $\sigma^2_{\mu_{eq}} \simeq \frac{1}{A^2}\frac{A}{A_{kN}}\sigma^2_{\mu\_A_k} = \frac{1}{A}\frac{\sigma^2_{\mu\_A_k}}{A_{kN}}$

Define $A_\mu = \frac{\sigma_{\mu\_A_k}}{\mu_N \sqrt{A_{kN}}}$ ⇒ $\sigma^2_{\frac{\mu_{eq}}{\mu_N}} = \frac{1}{A}\frac{\sigma^2_{\mu\_A_k}}{\mu_N^2 A_{kN}} = \frac{A_\mu^2}{A}$

Concept can be extended so now have:

$$\sigma^2_{\frac{\mu_R}{\mu_N}} = \frac{A_\mu^2}{WL}$$

$$\sigma^2_{\frac{C_{OXR}}{C_{OXN}}} = \frac{A_{Cox}^2}{WL}$$

$$\sigma^2_{V_{THR}} = \frac{A_{VT0}^2}{WL}$$

$$\sigma^2_{\frac{R}{R_N}} = \frac{A_{R\square}^2}{WL}$$

where A_μ,A_{Cox},A_{VT0} ,$A_{R\square}$ are Pelgrom process parameters

Statistical Simulations

Often simulations are used to predict statistical performance of a circuit

Variable of interest are often Gaussian (e.,g. R_R, C_R, V_{OSR}, I_R,….)

Most CAD tools do not have a rich set of random variable distributions (maybe not even the Gaussian distribution)

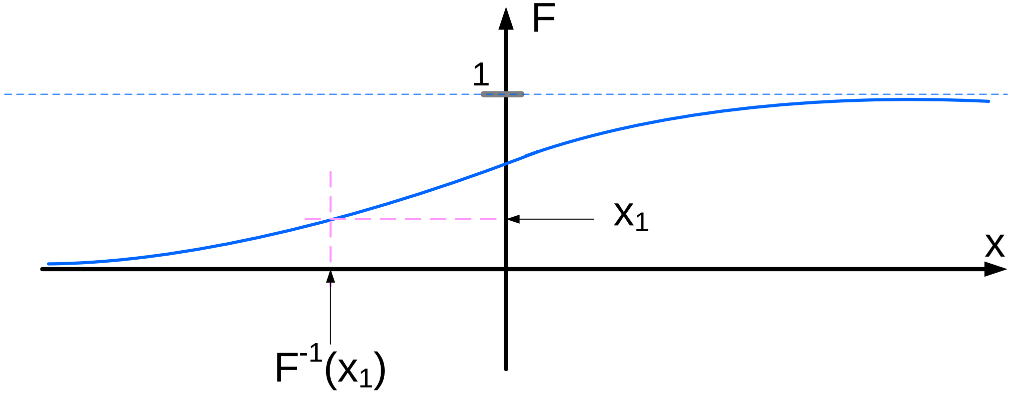
Many tools only have a single random variable generator that is U [0,1]

Theorem: f(y) and F(y) are any pdf/cdf pair and if X~ U[0,1], then $y = F^{-1}(x)$ has a pdf of f(y).

Corollary: If h is a rv with $F(h) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{h} e^{-\frac{x^2}{2}} dx$

then y=F^{-1}(h) is N[0,1]

CDF showing random variable mapping of x_1 from U(0,1)



Theorem: If y~N[0,1], then z = σy+μ is N[μ,σ]

$$F(h) = \frac{1}{2}\left[1 + \operatorname{erf}\left(\frac{h-\mu}{\sigma\sqrt{2}}\right)\right]$$

In Excel:

NORM.S.INV(h)=F^{-1}(h) where

$$F(h) = \int_{-\infty}^{h} \frac{1}{\sqrt{2\pi}} e^{-\frac{x^2}{2}} dx$$

NORM.DIST(h,μ,σ,TRUE) = f(h) where

$$f(h) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{h-\mu}{\sigma}\right)^2}$$

NORM.DIST(h,μ,σ,FALSE) = F(h) where

$$F(h) = \int_{-\infty}^{h} \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2} dx$$

Some useful relationships:

$$\mathrm{ERF}(x) = \frac{2}{\pi}\int_0^x e^{-t^2}\,dt$$

The CDF of the N(0,1) random variable x is given by

$$F_N(x) = \frac{1}{2}\left(1 + \mathrm{ERF}\left(\frac{x}{\sqrt{2}}\right)\right)$$

Excel	Older Excel	
@NORM.DIST		$f(x)$
@NORM.S.DIST		$f_N(x)$
@NORM.INV	@NORMINV	$F^{-1}(x)$
@NORM.S.INV	@NORMSINV	$F_N^{-1}(x)$
	@NORMDIST	$F_N(x)$
	@NORMINV	$F(x)$

where f: PDF F:CDF

Example: Determine the area required for the resistors for an n-bit R-string DAC to achieve a yield of P if the device is marketable provided $\left|INL_{kMAX}\right| < \frac{1}{2}LSB$

Solution:

Want: $$P = \int_{x=-\frac{1}{2}}^{x=+\frac{1}{2}} f\left(INL_{kMAX}\right)dx$$

Let $X_N = \dfrac{x}{\sigma_{INL_{kMAX}}}$ recall $\mu_{INL_{kMAX}} = 0$

$$\sigma_{INL_{kMAX}} = \frac{\sqrt{N}}{2}\sigma_{\frac{R_R}{R_N}}$$

$$\Rightarrow \quad X_N = \frac{\frac{1}{2}}{\frac{\sqrt{N}}{2}\sigma_{\frac{R_R}{R_N}}} = \frac{1}{\sqrt{N}\sigma_{\frac{R_R}{R_N}}}$$

thus $$P = \int_{-X_N}^{X_N} f_N\left(x\right)dx \qquad f_N \sim N\left(0,1\right)$$

Since P is fixed, can solve for X_N

$$P = 2F_N(X_N) - 1 \quad \Rightarrow \quad X_N = F_N^{-1}\left(\frac{P+1}{2}\right)$$

where $F_N(X_N)$ is the CDF of a N(0,1) rv

$$X_N = \frac{1}{\sigma_{\frac{R_R}{R_N}}\sqrt{N}}$$

recall

$$\sigma_{\frac{R_R}{R_N}} = \frac{A_R}{\sqrt{WL}}$$

thus

$$X_N = \frac{\sqrt{WL}}{A_R\sqrt{N}} \quad \Rightarrow \quad \sqrt{WL} = A_R\sqrt{N}X_N$$

thus, we obtain

$$\sqrt{WL} = A_R\sqrt{N} \bullet F_N^{-1}\left(\frac{P+1}{2}\right)$$

Since there are N=2^n resistors, total area becomes

$$A_{TOT} = 2^n WL = 2^n A_R^2 N \bullet \left(F_N^{-1}\left(\frac{P+1}{2} \right) \right)^2 = 2^{n+1} A_R^2 \bullet \left(F_N^{-1}\left(\frac{P+1}{2} \right) \right)^2$$

Summarizing:

$$A_{TOT} = 2^{n+1} A_R^2 \bullet \left(F_N^{-1}\left(\frac{P+1}{2} \right) \right)^2$$

Offset Voltages

All ADCs have comparators and many ADCs and DACs have operational amplifiers

The offset voltages of both amplifiers and comparators are random variables and invariably are key factors affecting the performance of a data converter

Operational Amplifiers:

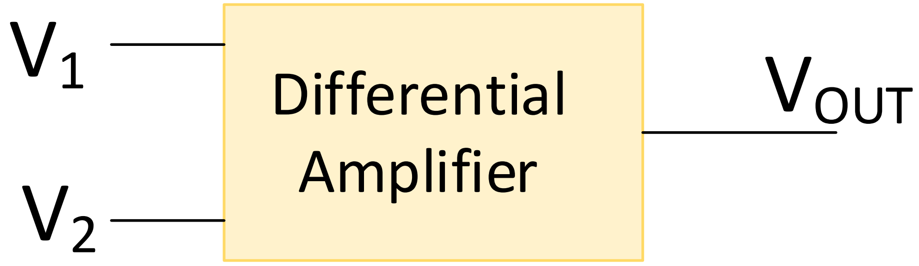
Generally differential amplifiers whose offset is dominantly determined by randomness in the first stage

Comparators:

High Gain Operational Amplifiers
Latching Structures (often clocked)
Combination of High Gain Amplifiers and Latching Structures

- Offset voltages of high-gain amplifiers well understood
- Offset voltage of Latching Structures often difficult to determine and can be very large

Consider First Offset in Operational Amplifiers



Input-referred Offset Voltage: Differential Voltage that must be applied to the input to make the output assume its <u>desired value</u>

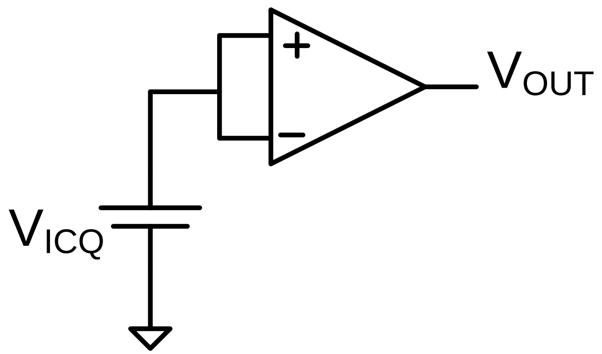
With a good design, a designer will have V_{OUT} at the desired value if the components assume the values used in the design

Any difference in the output from what is desired when components assume the nominal values used in a design is attributable to a systematic offset voltage

Offset Voltage

Two types of offset voltage:

- Systematic Offset Voltage
- Random Offset Voltage

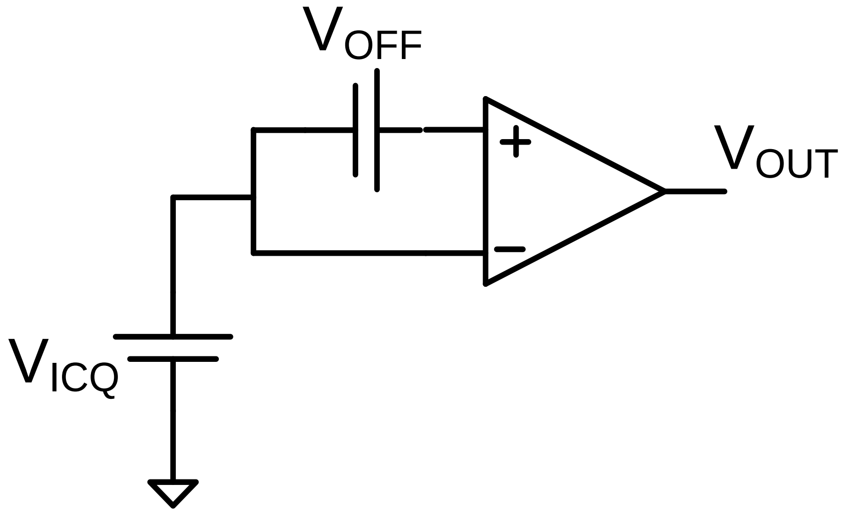


Definition: The output offset voltage is the difference between the desired output and the actual output when V_{id}=0 and V_{ic} is the quiescent common-mode input voltage.

$$V_{OUTOFF} = V_{OUT} - V_{OUTDES}$$

Note: V_{OUTOFF} is dependent upon V_{ICQ} although this dependence is usually quite weak and often not specified

Offset Voltage



Definition: The input-referred offset voltage is the differential dc input voltage that must be applied to obtain the desired output when V_{ic} is the quiescent common-mode input voltage.

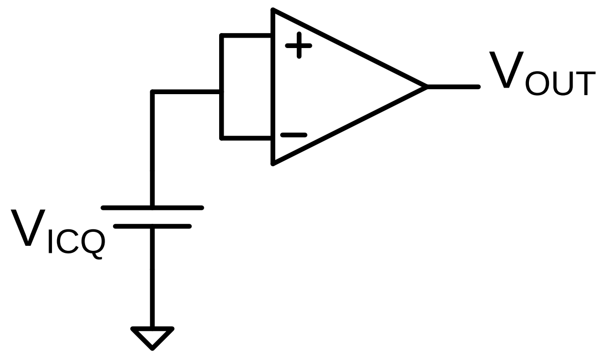
Note: V_{OFF} is usually related to the output offset voltage by the expression

$$V_{OFF} = \frac{V_{OUTOFF}}{A_D}$$

Note: V_{OFF} is dependent upon V_{ICQ} although this dependence is usually quite weak and often not specified

Offset Voltage

- Systematic Offset Voltage
- Random Offset Voltage



After fabrication it is impossible (difficult) to distinguish between the systematic offset and the random offset in any individual op amp

Measurements of offset voltages for a large number of devices will provide mechanism for identifying systematic offset and statistical characteristics of the random offset voltage

Systematic Offset Voltage

Offset voltage that is present if all device and model parameters assume their nominal value

Easy to simulate the systematic offset voltage

Almost always the designer's responsibility to make systematic offset voltage very small

Generally easy to make the systematic offset voltage small

Can tweak out systematic offset after design is almost done

Random Offset Voltage

Due to random variations in process parameters and device dimensions

Random offset is actually a random variable at the design level but deterministic after fabrication in any specific device

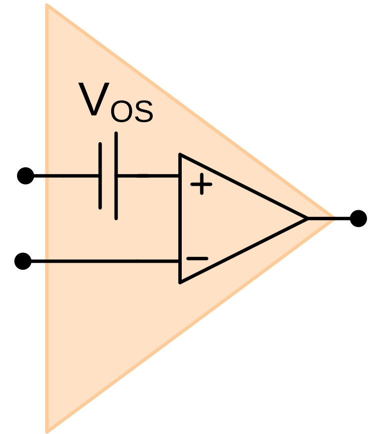
Distribution of native offset nearly Gaussian (If offset compensation is not employed)

Has zero mean

Characterized by its standard deviation or variance

Often strongly layout and area dependent

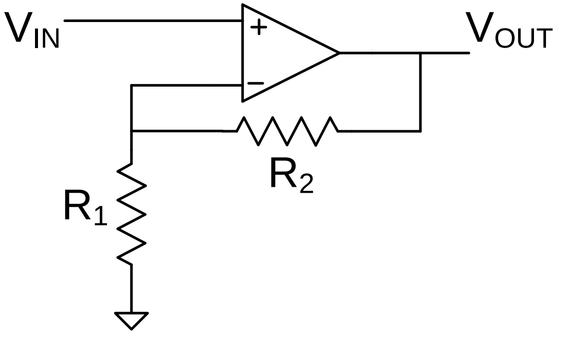
Offset Voltage



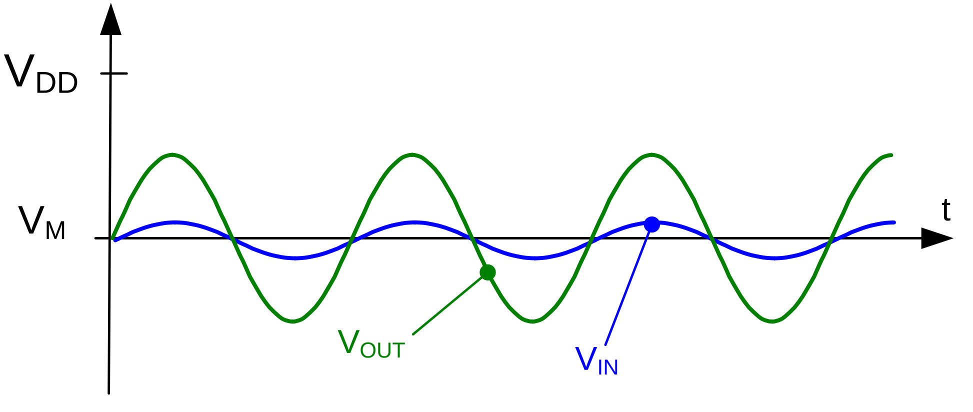
Can be modeled as a dc voltage source in series with the input (on either terminal)

Offset Voltage

Effects of Offset Voltage - <u>an example</u>

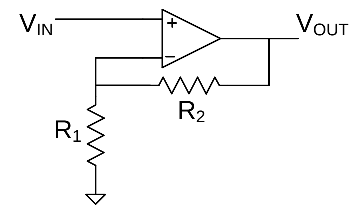


Desired I/O relationship

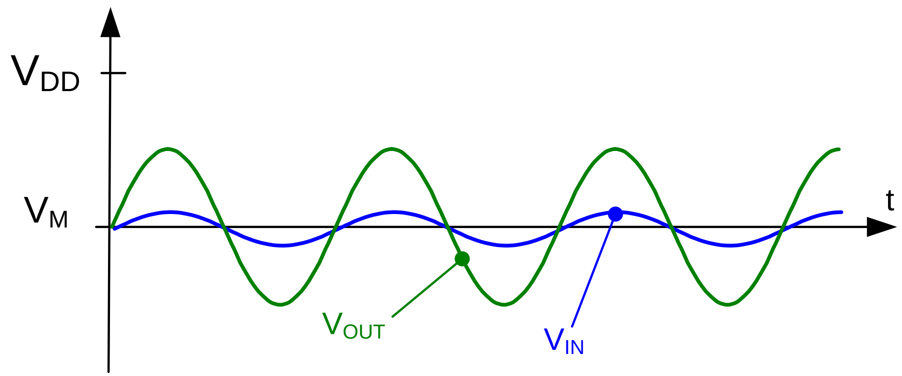


Offset Voltage

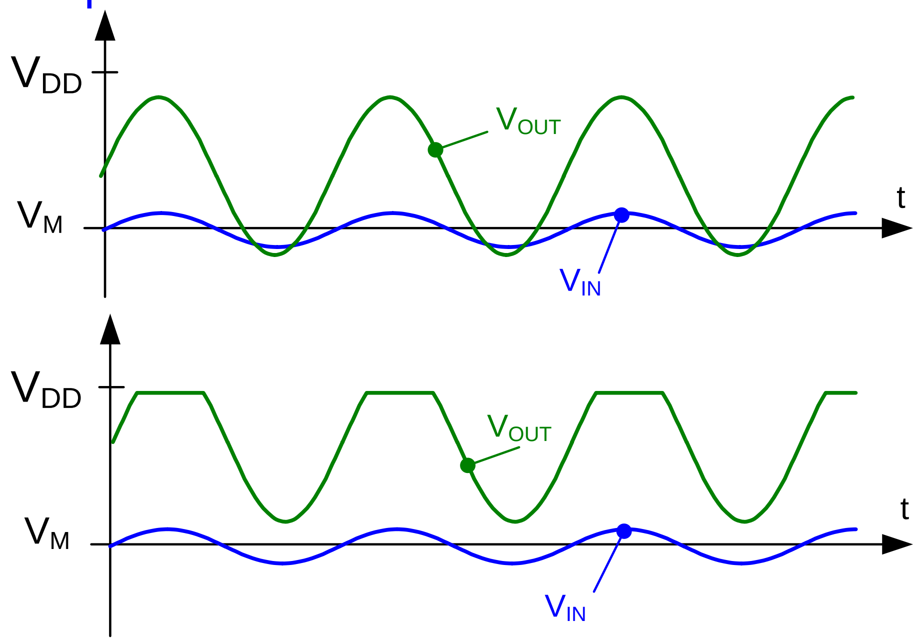
Effects of Offset Voltage - an example



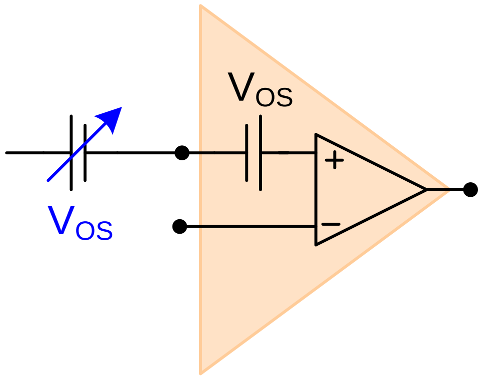
Desired I/O relationship



Actual I/O relationship due to offset



Offset Voltage



Effects can be reduced or eliminated by adding equal amplitude opposite phase DC signal (many ways to do this)

One such technique is “dynamic offset compensation”

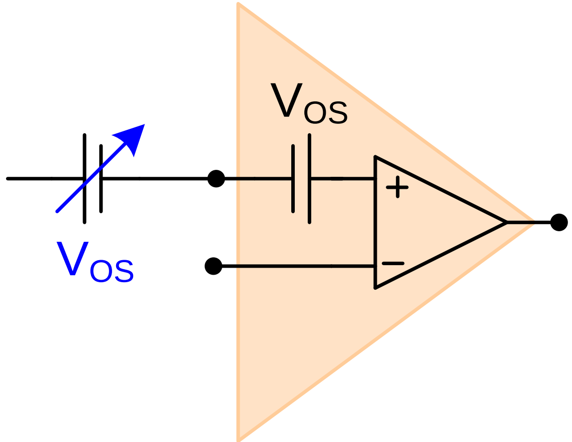
Another is chopper stabilization

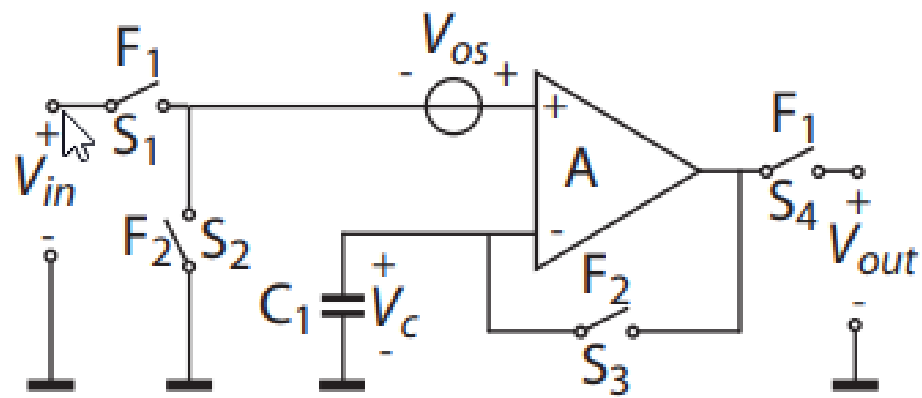
Widely used in offset-critical applications

Comes at considerable effort and expense

Prefer to have designer make V_{OS} small in the first place though penalty (e.g. cost) for making it sufficiently small without correction is often unacceptable

Dynamic Offset Compensation





Most basic dynamic offset compensation at input

Effects of Offset Voltage

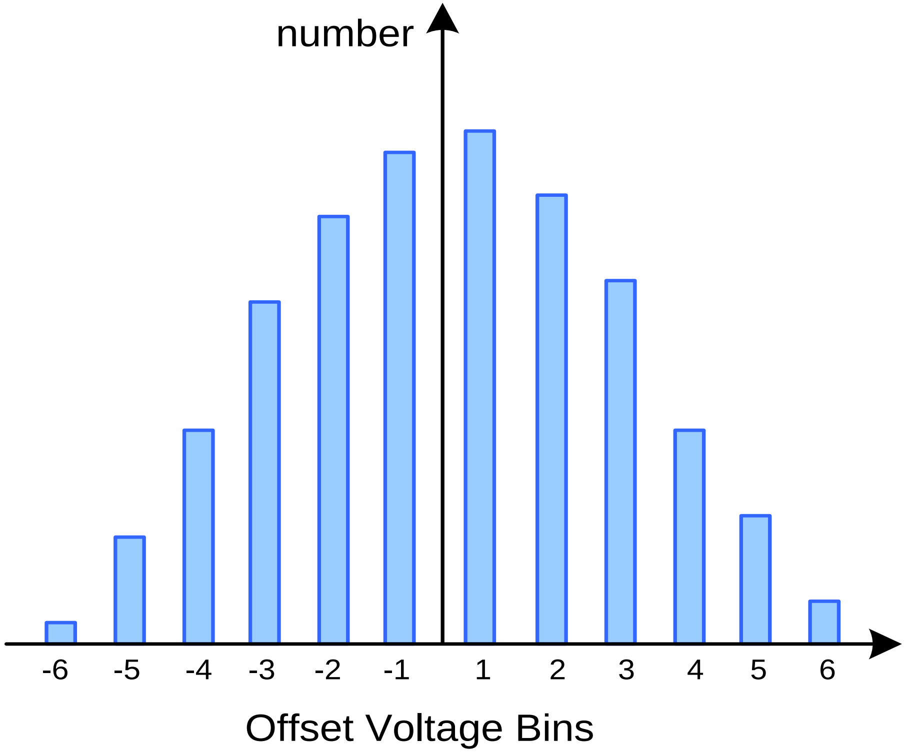
- Deviations in performance will change from one instantiation to another due to the random component of the offset

- Particularly problematic in high-gain circuits

- A major problem in many other applications

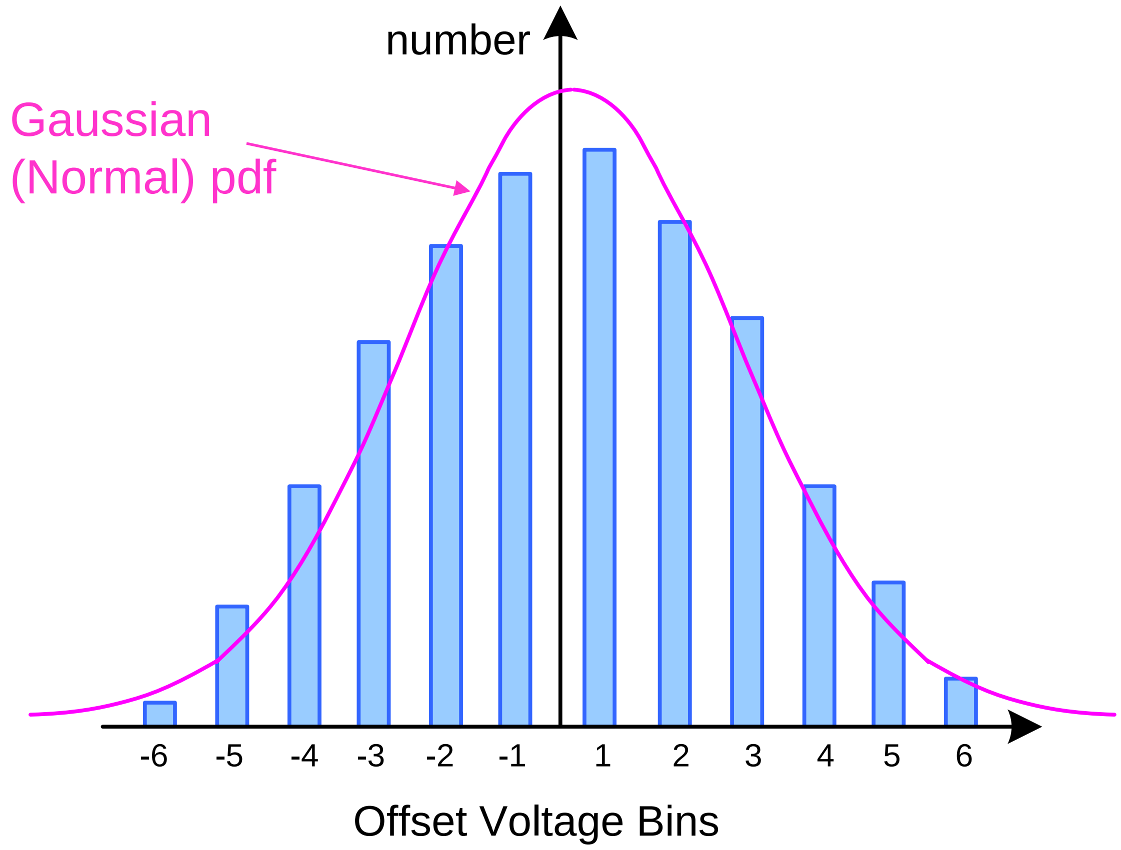
- Not of concern in many applications as well

Offset Voltage Distribution



Typical histogram of native offset voltage (binned) after fabrication

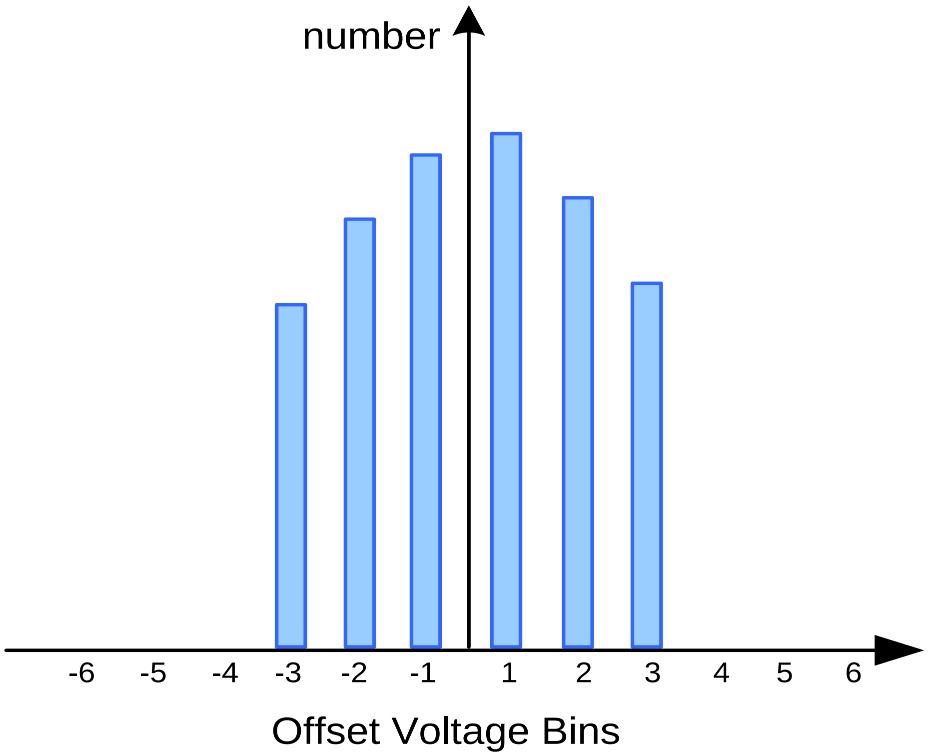
Offset Voltage Distribution



Typical histogram of offset voltage (binned) after fabrication

Mean is nearly 0 (actually the systematic offset voltage)

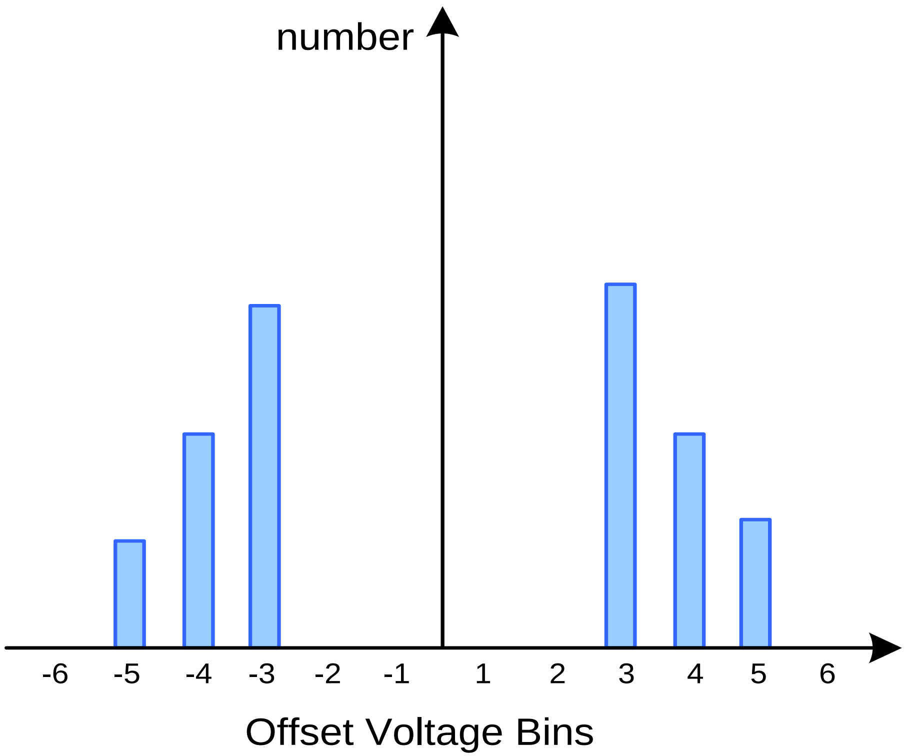
Offset Voltage Distribution



Typical histogram of offset voltage (binned) in shipped parts when entire population used for a single produce

Extreme offset parts have been sifted at test

Offset Voltage Distribution



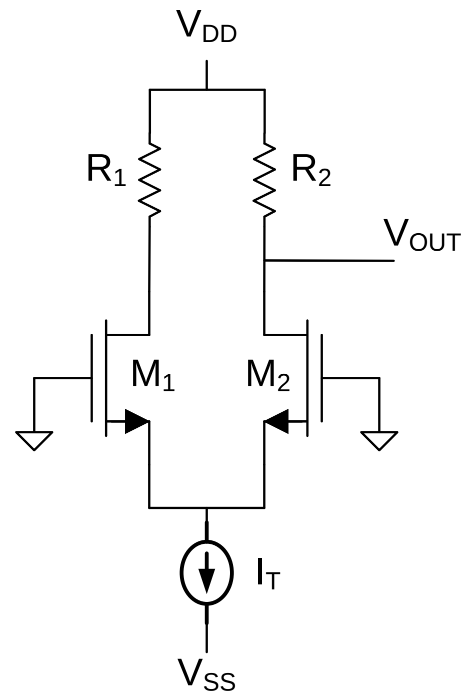
Typical histogram of offset voltage (binned) in shipped parts

Low-offset parts sold at a premium

Extreme offset parts have been sifted at test

Source of Random Offset Voltages

Consider as an example:



Ideally $R_1=R_2=R_N$, M_1 and M_2 are matched

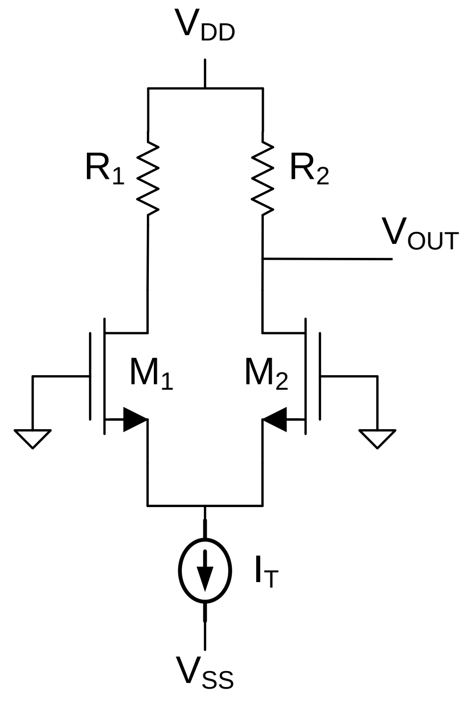
$$V_{OUT} = V_{DD} - \left(\frac{I_T}{2}\right) R_N$$

Assume this is the desired output voltage (note not assuming $V_{OUT\text{-}DES}$=0V)

Assume V_{INCOM}=0V (could consider different common-mode inputs)

Source of Random Offset Voltages

Consider as an example:



If everything ideal except R_1 and R_2

$$R_1=R_N+R_{R1} \quad R_2=R_N+R_{R2}$$

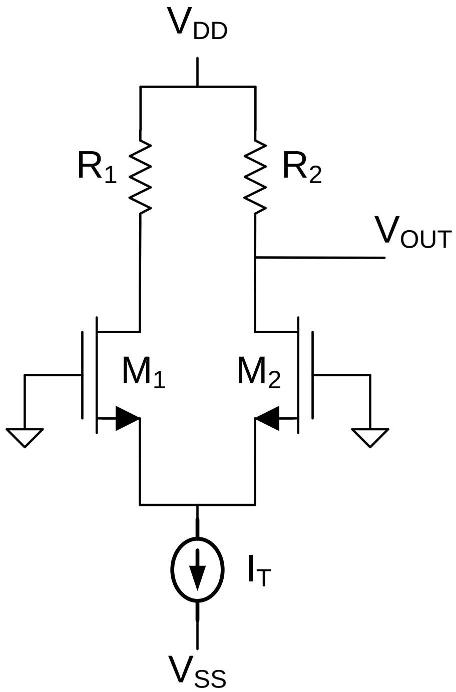
Thus at the design stage, V_{OUT} is also a random variable

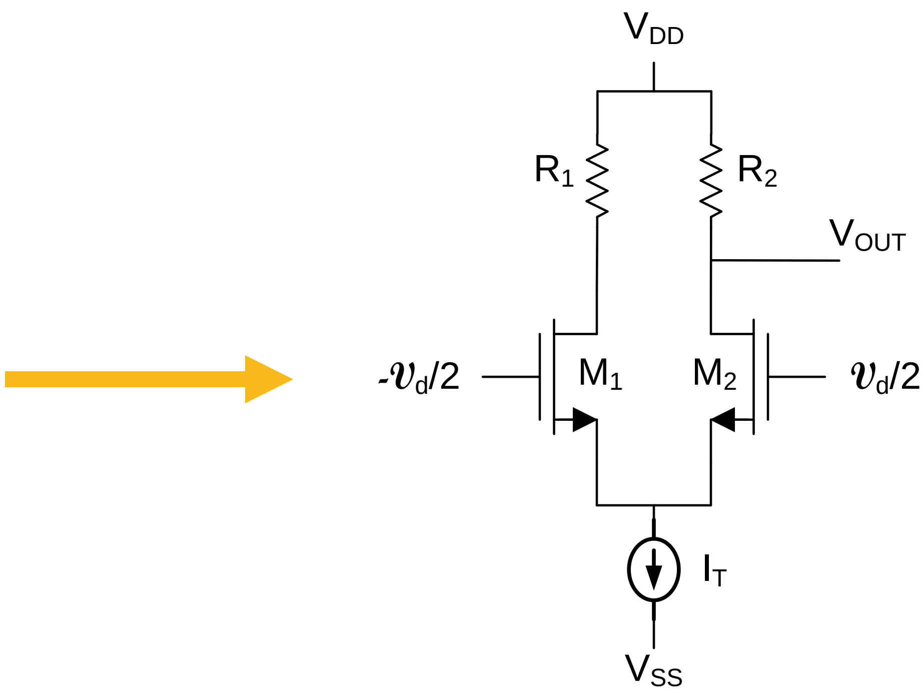
$$V_{OUT} = V_{DD}-\left(\frac{I_T}{2}\right)\left[R_N+R_{R2}\right]$$

$$V_{OUT-R} = -\left(\frac{I_T}{2}\right)R_{R2}$$

Source of Random Offset Voltages

Consider as an example:

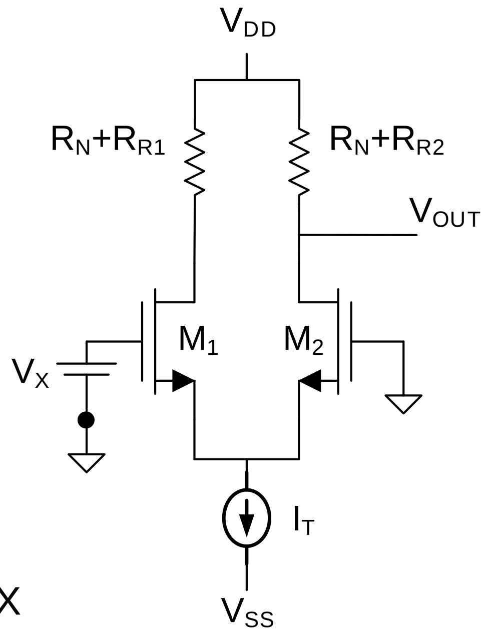




$$A_{VN} = -\frac{g_m}{2} R_N$$

Source of Random Offset Voltages

Determine the offset voltage – i.e. value of V_X needed to obtain desired output



$$A_V = -\frac{g_m}{2} R_N$$

$$V_{OUT} = \left[V_{DD} - \left(\frac{I_T}{2}\right) R_N \right] - \left(\frac{I_T}{2}\right) R_{R2} - A_V V_X$$

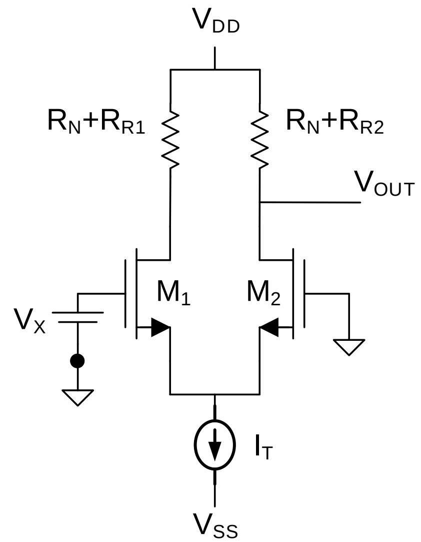
$$V_{OUT\text{-}DES} = \left[V_{DD} - \left(\frac{I_T}{2}\right) R_N \right]$$

Setting $V_{OUT}=V_{OUT\text{-}DES}$ and solving for V_X, we obtain

$$V_X = V_{OFF} = \frac{-1}{A_V}\left(\frac{I_T}{2}\right) R_{R2}$$

Source of Random Offset Voltages

Determine the offset voltage – i.e. value of V_X needed to obtain desired output



$$A_V = -\frac{g_m}{2}R$$

$$V_X = V_{OFF} = \frac{-1}{A_V}\left(\frac{I_T}{2}\right)R_{R2}$$

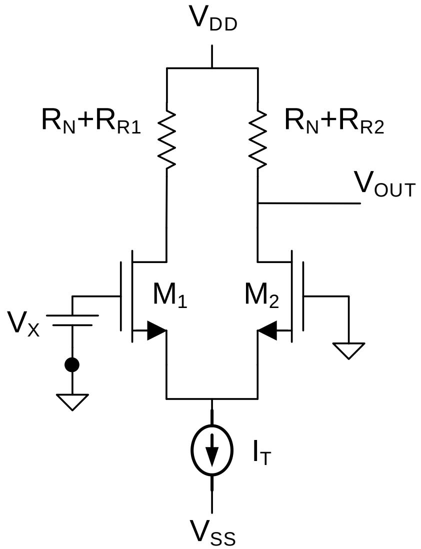
$$V_X = \frac{2}{g_m R_N}\left(\frac{I_T}{2}\right)R_{R2} = \left(\frac{I_T}{g_m}\right)\frac{R_{R2}}{R_N} = \left(\frac{I_T}{I_T/V_{EB}}\right)\frac{R_{R2}}{R_N} = V_{EB}\frac{R_{R2}}{R_N}$$

$$V_{OFF} = V_{EB}\frac{R_{R2}}{R_N}$$

As conjectured, V_{OFF} is a random variable!

Source of Random Offset Voltages

Determine the offset voltage – i.e. value of V_X needed to obtain desired output



$$V_{OFF} = V_{EB}\frac{R_{R2}}{R_N}$$

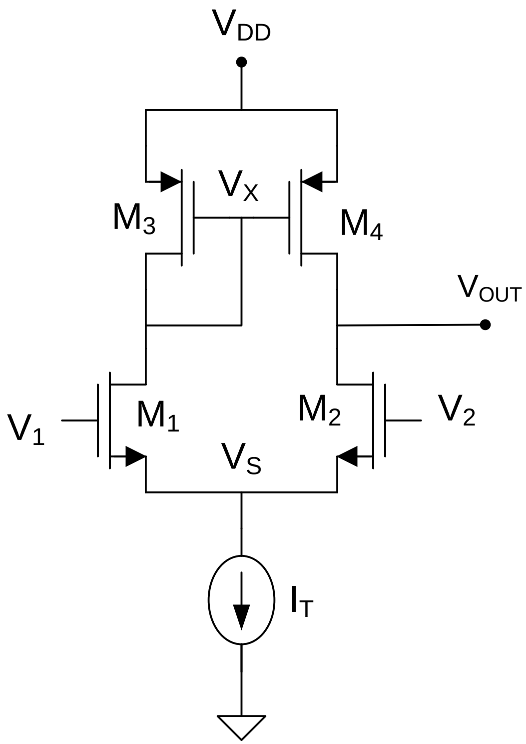
$$\sigma_{V_{OFF}} = V_{EB}\sigma_{\frac{R_{R2}}{R_N}}$$

If resistors are integrated and A is the resistor area $\sigma_{\frac{R_{R2}}{R_N}} = \frac{A_R}{\sqrt{A}}$ where A_R is the Pelgrom parameter

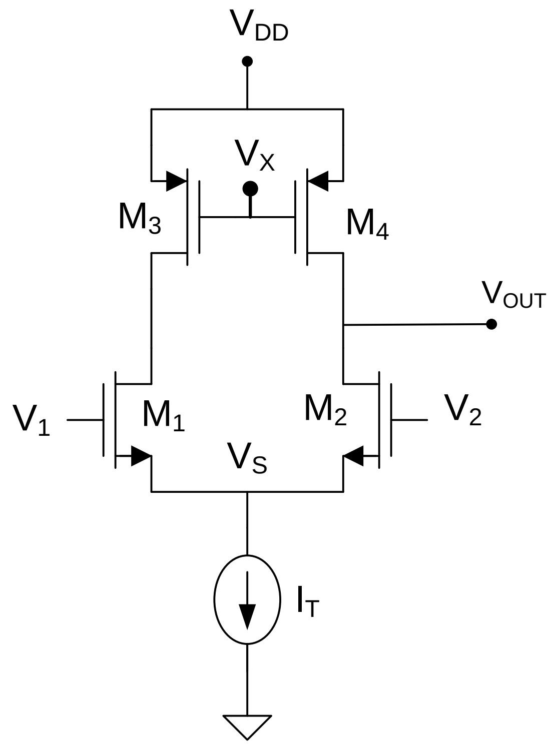
Thus $\sigma_{V_{OFF}} = V_{EB}\frac{A_R}{\sqrt{A}}$

Source of Random Offset Voltages

The random offset voltage is almost entirely that of the input stage in most op amps

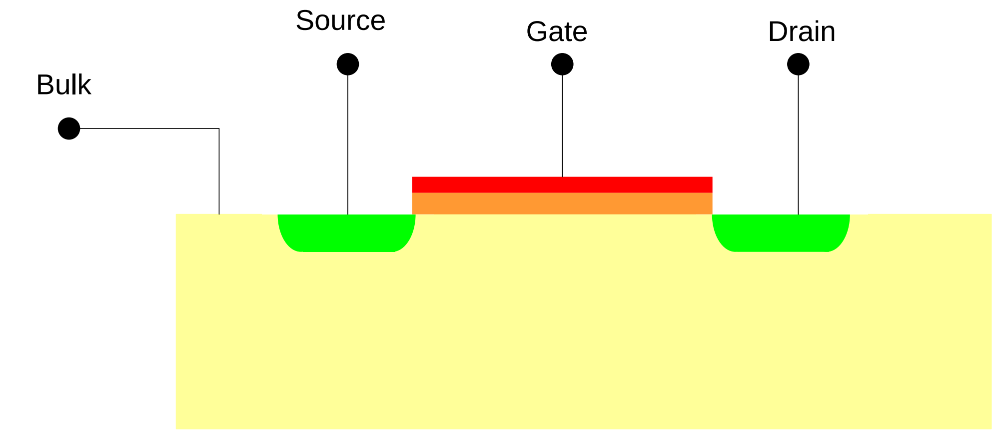


(a)

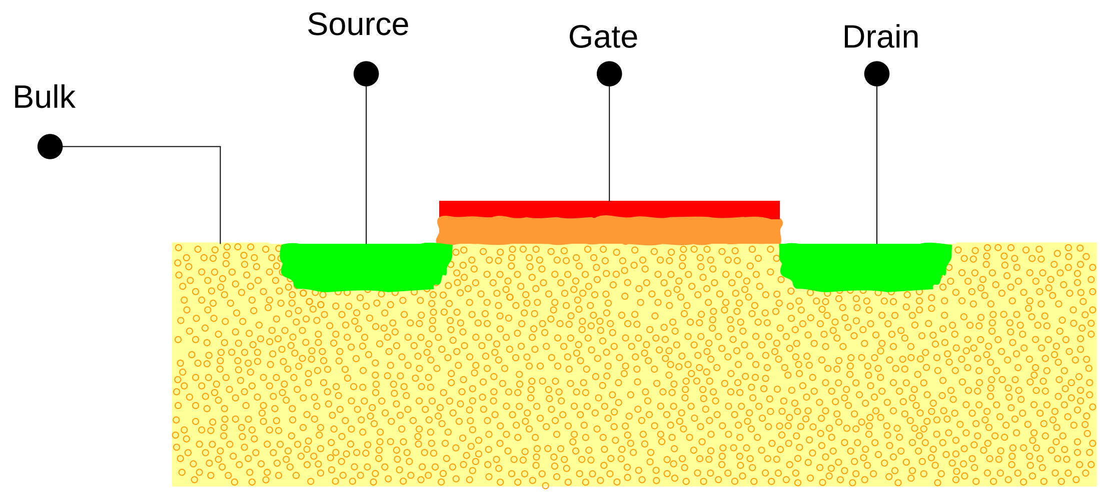


(b)

Random Offset Voltages



n-channel MOSFET

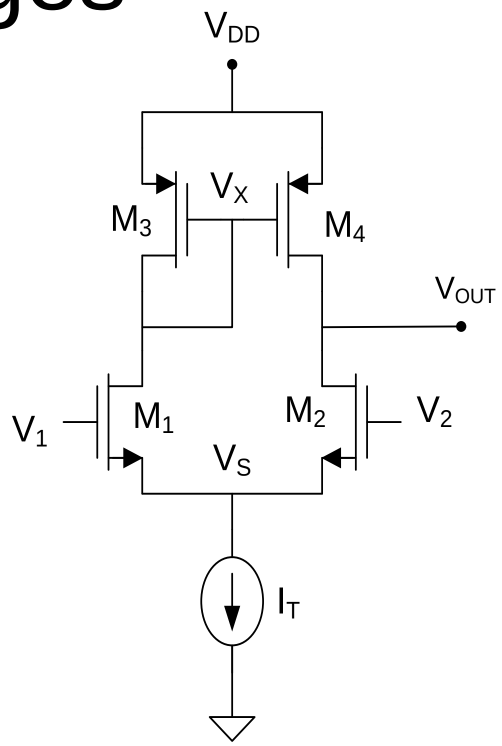


n-channel MOSFET

Impurities vary randomly with position as do edges of gate, oxide and diffusions

Model and design parameters vary throughout channel and thus the corresponding equivalent lumped model parameters will vary from device to device

Random Offset Voltages



The random offset is due to missmatches in the four transistors, dominantly missmatches in the parameters {V_T, μ,C_{OX},W and L}

The relative missmatch effects become more pronounced as devices become smaller

$$V_{Ti}=V_{TN}+V_{TRi}$$

$$C_{OXi}=C_{OXN}+C_{OXRi}$$

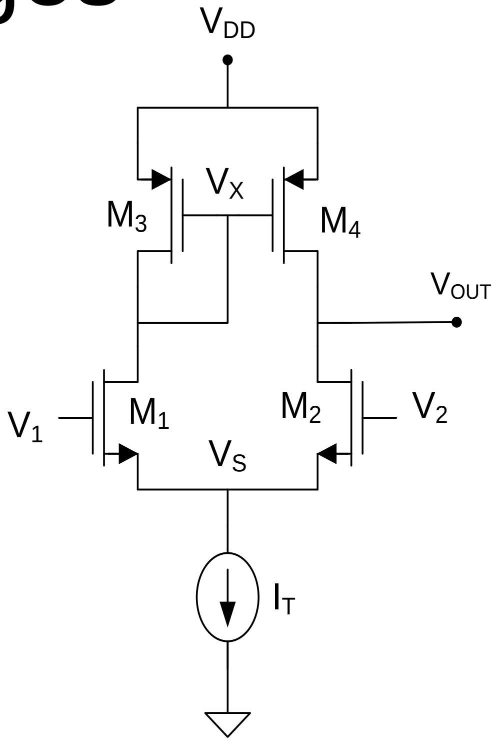
$$\mu_i=\mu_N+\mu_{Ri}$$

$$W_i=W_N+W_{Ri}$$

$$L_i=L_N+L_{Ri}$$

Each design and model parameter is comprised of a nominal part and a random component

Random Offset Voltages



$$V_{Ti}=V_{TN}+V_{TRi}$$

$$C_{OXi}=C_{OXN}+C_{OXRi}$$

$$\mu_i=\mu_N+\mu_{Ri}$$

$$W_i=W_N+W_{Ri}$$

$$L_i=L_N+L_{Ri}$$

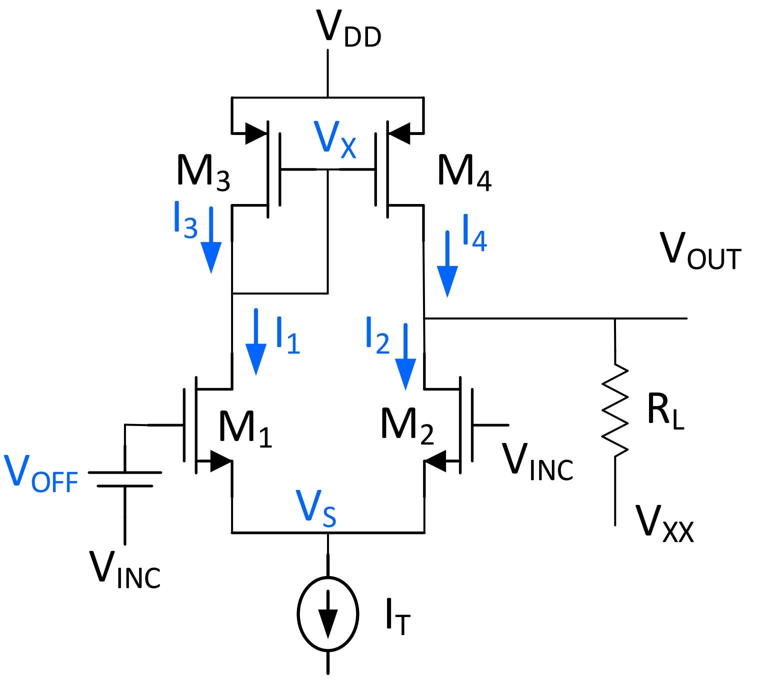
For each device, the device model is often expressed as

$$I_{Di} = \frac{(\mu_N+\mu_{Ri})(C_{OXN}+C_{OXRi})(W_N+W_{Ri})}{2(L_N+L_{Ri})}\left(V_{GSi}-(V_{TN}+V_{TRi})\right)^2\left(1+(\lambda_N+\lambda_{Ri})[V_{DS}]\right)$$

Because of the random components of the parameters in every device, matching from the left-half circuit to the right half-circuit is not perfect

This mismatch introduces an offset voltage which is a random variable

Offset Voltages



Assume currents at output node must satisfy relation $I_2=I_4$

(this is equivalent to assuming desired output voltage is V_{XX} in this circuit)

Strategy:

1) Obtain expression for V_{OFF} (referred to input) that forces $I_2=I_4$
2) Linearize expression in terms of design variables and decorrelate
3) Obtain σ_{VOS}

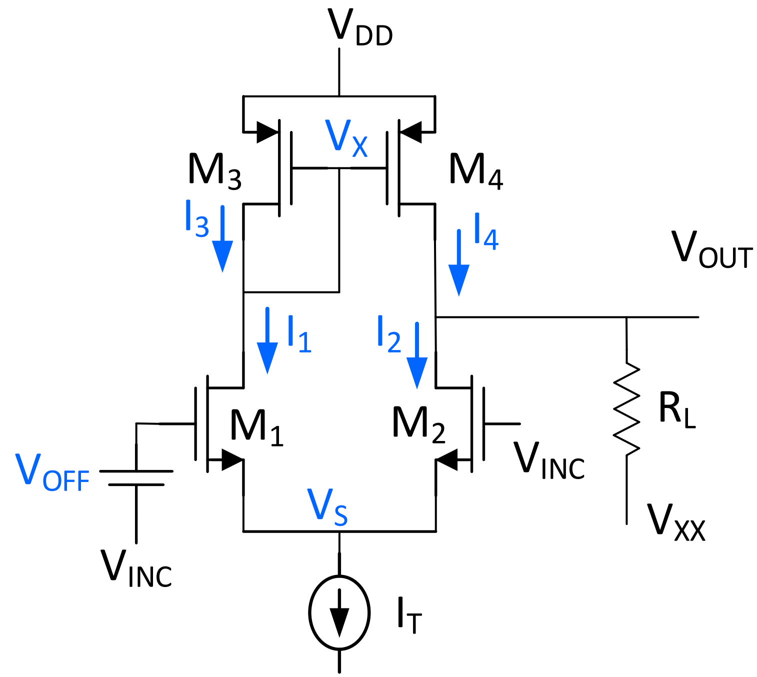
Analysis of Offset Voltage (Neglect R_L)

$$I_{D1}=\frac{\mu_{n1}C_{OX1}W_1}{2L_1}\left(V_{OFF}+V_{INC}-V_S-V_{TH1}\right)^2$$

$$I_{D2}=\frac{\mu_{n2}C_{OX2}W_2}{2L_2}\left(V_{INC}-V_S-V_{TH2}\right)^2$$

$$I_{D3}=\frac{\mu_{p3}C_{OX3}W_3}{2L_3}\left(V_X-V_{DD}-V_{TH3}\right)^2$$

$$I_{D4}=\frac{\mu_{p4}C_{OX4}W_4}{2L_4}\left(V_X-V_{DD}-V_{TH4}\right)^2$$



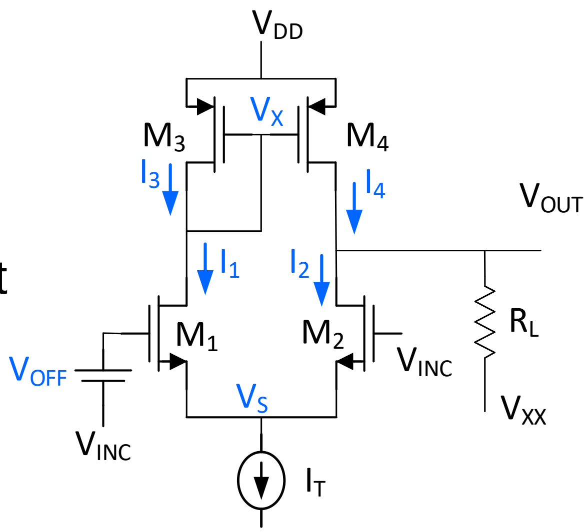
Since $\sqrt{I_{D1}}=\sqrt{I_{D3}}$

$$V_{OFF}+V_{INC}-V_S-V_{TH1}=\sqrt{\frac{\mu_{p3}C_{OX3}W_3L_1}{\mu_{n1}C_{OX1}W_1L_3}}\left(V_X-V_{DD}-V_{TH3}\right)$$

Since $\sqrt{I_{D2}}=\sqrt{I_{D4}}$

$$V_{INC}-V_S-V_{TH2}=\sqrt{\frac{\mu_{p4}C_{OX4}W_4L_2}{\mu_{n2}C_{OX2}W_2 2L_4}}\left(V_X-V_{DD}-V_{TH4}\right)$$

Analysis of Offset Voltage



Define:

$$a = \sqrt{\frac{L_1\mu_{p3}C_{OX3}W_3}{L_3\mu_{n1}C_{OX1}W_1}} \qquad b = \sqrt{\frac{L_2\mu_{p4}C_{OX4}W_4}{L_4\mu_{n2}C_{OX2}W_2}}$$

Substituting for a and b, it follows on eliminating V_S that

$$V_{OFF} = V_{TH1} - V_{TH2} + (a-b)(V_X - V_{DD}) + bV_{TH4} - aV_{TH3}$$

Assume

$$V_X = V_{XN} - V_{XR}$$
$$a = a_N + a_R$$
$$b = b_N + b_R$$
$$V_{Tni} = V_{TnN} + V_{TnRi} \qquad i = 1,2$$
$$V_{Tpi} = V_{TpN} + V_{TpRi} \qquad i = 3,4$$

Observe $a_N = b_N$ and $V_{XN} - V_{DD} - V_{TpN} = V_{EB3N}$

Since the random part of V_X multiplies only a-b which is small, it follows that

$$V_{OFF} = V_{TH1} - V_{TH2} + (a-b)(V_{EB3N}) + bV_{TH4} - aV_{TH3}$$

$$V_{OFF} = V_{THR1} - V_{THR2} + (a_R - b_R)V_{EB3N} + a_N(V_{THR4} - V_{THR3})$$

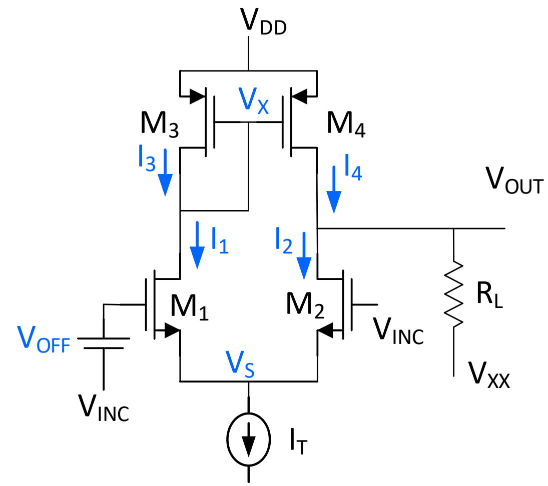
$$\sigma^2_{V_{OFF}} = 2\sigma^2_{V_{TnR}} + a_N^2 2\sigma^2_{V_{TpR}} + V^2_{EB3N}\sigma^2_{V_{a_R-b_R}}$$

Will now obtain a_R and b_R

Analysis of Offset Voltage

$$V_{OFF} = V_{TnR2} - V_{TnR2} + (b_R - a_R)V_{EB3} + a_N\left(V_{TpR3} - V_{TpR4}\right)$$

$$a = \sqrt{\frac{(L_{N1}+L_{R1})(\mu_{Np3}+\mu_{R3})(C_{OXN3}+C_{OXR3})(W_{N3}+W_{R3})}{(L_{N3}+L_{R3})(\mu_{Nn1}+\mu_{R1})(C_{OXN1}+C_{OXR1})(W_{N1}+W_{R1})}}$$



Recall for x small, $\sqrt{1+x} \cong 1 + \frac{x}{2}$ $\quad \frac{1}{1+x} \cong 1 - x$

$$a = \sqrt{\frac{(L_{N1}\mu_{Np3}W_{N3})}{(L_{N3}\mu_{Nn1}W_{N1})}}\left(1 + \frac{1}{2}\left[\frac{L_{R1}}{L_{N1}} - \frac{L_{R3}}{L_{N3}} + \frac{\mu_{R3}}{\mu_{Np3}} - \frac{\mu_{R1}}{\mu_{Nn1}} + \frac{C_{OXR3}}{C_{OXN3}} - \frac{C_{OXR1}}{C_{OXN1}} + \frac{W_{R3}}{W_{N3}} - \frac{W_{R3}}{W_{N3}}\right]\right)$$

Thus

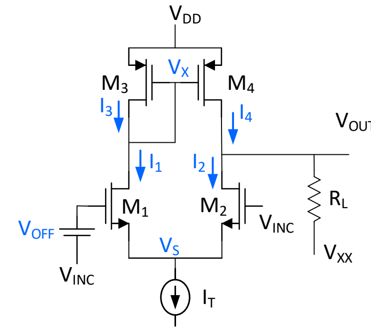
$$a_R = \sqrt{\frac{(L_{N1}\mu_{Np3}W_{N3})}{(L_{N3}\mu_{Nn1}W_{N1})}}\frac{1}{2}\left[\frac{L_{R1}}{L_{N1}} - \frac{L_{R3}}{L_{N3}} + \frac{\mu_{R3}}{\mu_{N3}} - \frac{\mu_{R1}}{\mu_{N1}} + \frac{C_{OXR3}}{C_{OXN3}} - \frac{C_{OXR1}}{C_{OXN1}} + \frac{W_{R3}}{W_{N3}} - \frac{W_{R3}}{W_{N3}}\right]$$

$$a_N = \sqrt{\frac{(L_{N1}\mu_{Np3}W_{N3})}{(L_{N3}\mu_{Nn1}W_{N1})}}$$

Likewise

$$b_R = \sqrt{\frac{(L_{N1}\mu_{Np3}W_{N3})}{(L_{N3}\mu_{Nn1}W_{N1})}}\frac{1}{2}\left[\frac{L_{R2}}{L_{N2}} - \frac{L_{R4}}{L_{N4}} + \frac{\mu_{R4}}{\mu_{Np4}} - \frac{\mu_{R2}}{\mu_{Nn2}} + \frac{C_{OXR4}}{C_{OXN4}} - \frac{C_{OXR2}}{C_{OXN2}} + \frac{W_{R4}}{W_{N4}} - \frac{W_{R2}}{W_{N2}}\right]$$

Analysis of Offset Voltage



$$a_R - b_R = \sqrt{\frac{(L_{N1}\mu_{Np3}W_{N3})}{(L_{N3}\mu_{Nn1}W_{N1})}}\,\frac{1}{2}\left[\frac{L_{R1}}{L_{N1}} - \frac{L_{R2}}{L_{N2}} + \frac{L_{R4}}{L_{N4}} - \frac{L_{R3}}{L_{N3}} + \frac{\mu_{R3}}{\mu_{Np3}} - \frac{\mu_{R4}}{\mu_{Np4}} + \frac{\mu_{R2}}{\mu_{Nn2}} - \frac{\mu_{R1}}{\mu_{Nn1}} + \frac{C_{OXR3}}{C_{OXN3}} - \frac{C_{OXR4}}{C_{OXN4}} + \frac{C_{OXR2}}{C_{OXN2}} - \frac{C_{OXR1}}{C_{OXN1}} + \frac{W_{R3}}{W_{N3}} - \frac{W_{R4}}{W_{N4}} + \frac{W_{R2}}{W_{N2}} - \frac{W_{R3}}{W_{N3}}\right]$$

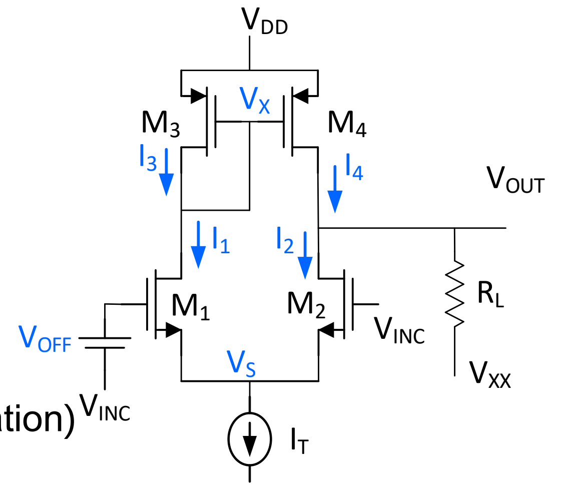
$$\sigma^2_{a_R - b_R} = \frac{(L_{N1}\mu_{Np3}W_{N3})}{(L_{N3}\mu_{Nn1}W_{N1})}\frac{1}{2}\left[\sigma^2_{\frac{L_{R1}}{L_{N1}}} + \sigma^2_{\frac{L_{R3}}{L_{N3}}} + \sigma^2_{\frac{\mu_{R3}}{\mu_{Np3}}} + \sigma^2_{\frac{\mu_{R2}}{\mu_{Nn2}}} + \sigma^2_{\frac{C_{OXR3}}{C_{OXN3}}} + \sigma^2_{\frac{C_{OXR1}}{C_{OXN1}}} + \sigma^2_{\frac{W_{R3}}{W_{N3}}} + \sigma^2_{\frac{W_{R1}}{W_{N1}}}\right]$$

Thus

$$\sigma^2_{V_{OFF}} = 2\sigma^2_{V_{TnR2}} + 2\frac{L_{N1}\mu_{Np3}W_{N3}}{L_{N3}\mu_{Nn1}W_{N1}}\sigma^2_{V_{TpR3}}$$

$$+V^2_{EB3N}\frac{(L_{N1}\mu_{Np3}W_{N3})}{(L_{N3}\mu_{Nn1}W_{N1})}\frac{1}{2}\left[\sigma^2_{\frac{L_{R1}}{L_{N1}}} + \sigma^2_{\frac{L_{R3}}{L_{N3}}} + \sigma^2_{\frac{\mu_{R3}}{\mu_{Np3}}} + \sigma^2_{\frac{\mu_{R2}}{\mu_{Nn2}}} + \sigma^2_{\frac{C_{OXR3}}{C_{OXN3}}} + \sigma^2_{\frac{C_{OXR1}}{C_{OXN1}}} + \sigma^2_{\frac{W_{R3}}{W_{N3}}} + \sigma^2_{\frac{W_{R1}}{W_{N1}}}\right]$$

Analysis of Offset Voltage



but

$$\sigma_{V_T}^2 = \frac{A_{VT0}^2}{WL} \qquad \sigma_{\frac{\mu_R}{\mu_N}}^2 = \frac{A_{\mu}^2}{WL} \qquad \sigma_{\frac{C_{OXR}}{C_{OXN}}}^2 = \frac{A_{Cox}^2}{WL} \qquad \sigma_{\frac{L_R}{L_N}}^2 = \frac{2A_L^2}{WL^2} \qquad \sigma_{\frac{W_R}{W_N}}^2 = \frac{2A_W^2}{W^2L}$$

So the offset variance can be expressed as (dropping the "N"notation)

$$\sigma_{V_{OFF}}^2 = 2\frac{A_{VTn0}^2}{W_1L_1} + 2\frac{\mu_p L_1}{\mu_n W_1}\frac{A_{VTp0}^2}{L_3^2}$$
$$+V_{EB3}^2\frac{\mu_p L_1 W_3}{\mu_n L_3 W_1}\frac{1}{2}\left[\frac{A_{\mu_n}^2}{W_3L_3} + \frac{A_{\mu_p}^2}{W_1L_1} + A_{Cox}^2\left(\frac{1}{W_3L_3}+\frac{1}{W_1L_1}\right) + A_W^2\left(\frac{2}{W_3^2L_3}+\frac{2}{W_1^2L_1}\right) + A_L^2\left(\frac{2}{W_1L_1^2}+\frac{2}{W_3L_3^2}\right)\right]$$

Often this can be approximated by

$$\sigma_{V_{OFF}}^2 = 2\frac{A_{VTn0}^2}{W_1L_1} + 2\frac{\mu_p L_1}{\mu_n W_1}\frac{A_{VTp0}^2}{L_3^2} + V_{EB3}^2\frac{\mu_p L_1 W_3}{\mu_n L_3 W_1}\frac{1}{2}\left[\frac{A_{\mu_n}^2}{W_3L_3} + \frac{A_{\mu_p}^2}{W_1L_1} + A_{Cox}^2\left(\frac{1}{W_3L_3}+\frac{1}{W_1L_1}\right)\right]$$

Or even approximated by

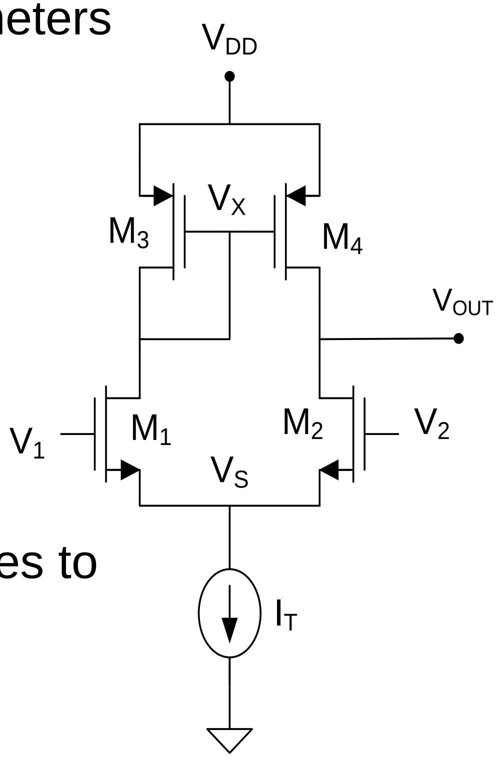
$$\sigma_{V_{OFF}}^2 = 2\frac{A_{VTn0}^2}{W_1L_1} + 2\frac{\mu_p L_1}{\mu_n W_1}\frac{A_{VTp0}^2}{L_3^2}$$

Random Offset Voltages

Since V_{EBn} and V_{EBp} are related, this is often expressed in simpler form as:

$$\sigma^2_{V_{OS}} = 2\left[\frac{A^2_{VTOn}}{W_nL_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_nL_p^2}A^2_{VTOp} + \frac{V^2_{EBn}}{4}\left(\frac{1}{W_nL_n}A^2_{\mu_n} + \frac{1}{W_pL_p}A^2_{\mu_p} + A^2_{COX}\left[\frac{1}{W_nL_n}+\frac{1}{W_pL_p}\right] + 2A^2_L\left[\frac{1}{W_nL_n^2}+\frac{1}{W_pL_p^2}\right] + A^2_W\left[\frac{1}{L_nW_n^2}+\frac{1}{L_pW_p^2}\right]\right)\right]$$

where the terms A_{VT0}, A_μ, A_{COX}, A_L, and A_W are process parameters



Representative values of Pelgrom parameters (0.5μ process)

$$A_{VT0} \simeq \begin{cases} 21\text{mV}\cdot\mu & \text{(n-ch)} \\ 25\text{mV}\cdot\mu & \text{(p-ch)} \end{cases}$$

$$\sqrt{A^2_\mu + A^2_{C_{OX}}} \simeq \begin{cases} .016\mu & \text{(n-ch)} \\ .023\mu & \text{(p-ch)} \end{cases}$$

$$A_L = A_W \simeq 0.017\mu^{3/2}$$

Usually the A_{VT0} terms are dominant, thus the variance simplifies to

$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTOn}}{W_nL_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_nL_p^2}A^2_{VTOp}\right]$$

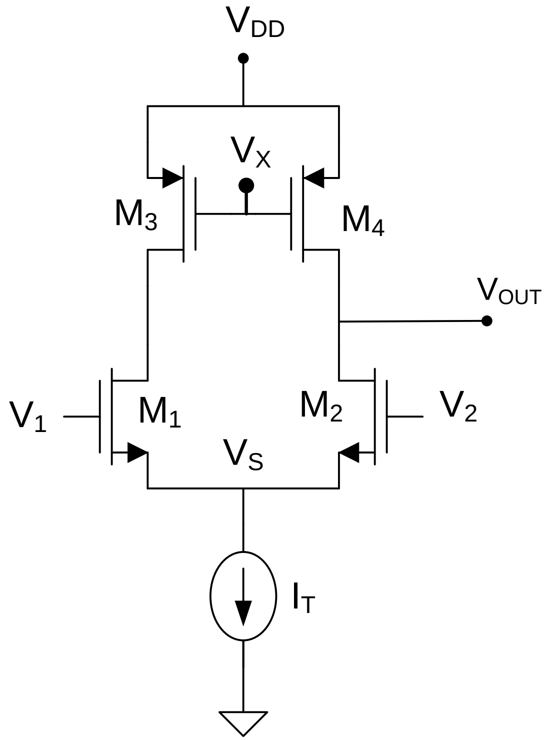
Random Offset Voltages

Correspondingly for 5T op amp w/o current mirror load:

$$\sigma_{V_{OS}}^2 = 2\left[\frac{A_{VTOn}^2}{W_nL_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_nL_p^2}A_{VTOp}^2 + \frac{V_{EBn}^2}{4}\left(\frac{1}{W_nL_n}A_{\mu_n}^2 + \frac{1}{W_pL_p}A_{\mu_p}^2 + A_{COX}^2\left[\frac{1}{W_nL_n}+\frac{1}{W_pL_p}\right] + 2A_L^2\left[\frac{1}{W_nL_n^2}+\frac{1}{W_pL_p^2}\right] + A_w^2\left[\frac{1}{L_nW_n^2}+\frac{1}{L_pW_p^2}\right]\right)\right]$$

which again simplifies to

$$\sigma_{V_{OS}}^2 \cong 2\left[\frac{A_{VTO\,n}^2}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A_{VTO\,p}^2\right]$$



Note these offset voltage expressions are identical!

Random Offset Voltages

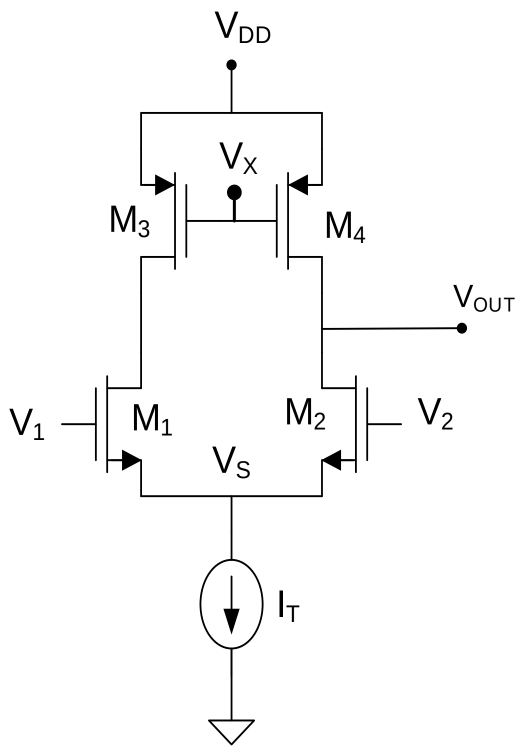
Example: Determine the 3σ value of the input offset voltage for the MOS differential amplifier if

a) M_1 and M_3 are minimum-sized and

b) the area of M_1 and M_3 are 100 times minimum size

Assume $L_{MIN}=W_{MIN}=0.5u$, $A_{VTOn}=0.021V$ and $A_{VTOP}=0.025V$

Will neglect μ_R, C_{OXR}, W_R and L_R on all devices



$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2} A^2_{VTO\,p}\right]$$

$$\sigma^2_{V_{OS}} \cong \frac{2}{W_n L_n}\left[A^2_{VTO\,n} + \frac{\mu_p}{\mu_n} A^2_{VTO\,p}\right]$$

a)

$$\sigma^2_{V_{OS}} \cong \frac{2}{(0.5\mu)^2}\left[.021^2 + \frac{1}{3}.025^2\right]$$

$$\sigma_{V_{OS}} \cong 72\text{mV}$$

$$3\,\sigma_{V_{OS}} \cong 216\text{mV}$$

Note this is a very large offset voltage !

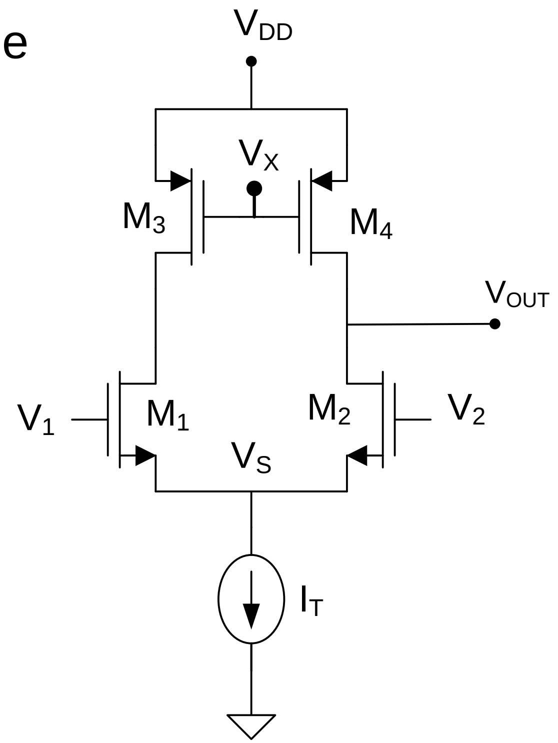
Random Offset Voltages

Example: Determine the 3σ value of the input offset voltage for the MOS differential amplifier if

a) M_1 and M_3 are minimum-sized and

b) the area of M_1 and M_3 are 100 times minimum size

Assume $L_{MIN}=W_{MIN}=0.5u$, $A_{VTOn}=0.021V$ and $A_{VTOP}=0.025V$



$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTOn}}{W_nL_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_nL_p^2}A^2_{VTOp}\right]$$

$$\sigma^2_{V_{OS}} \cong \frac{2}{W_nL_n}\left[A^2_{VTOn} + \frac{\mu_p}{\mu_n}A^2_{VTOp}\right]$$

b)

$$\sigma^2_{V_{OS}} \cong \frac{2}{\left[100(0.5\mu)\right]^2}\left[.021^2 + \frac{1}{3}.025^2\right]$$

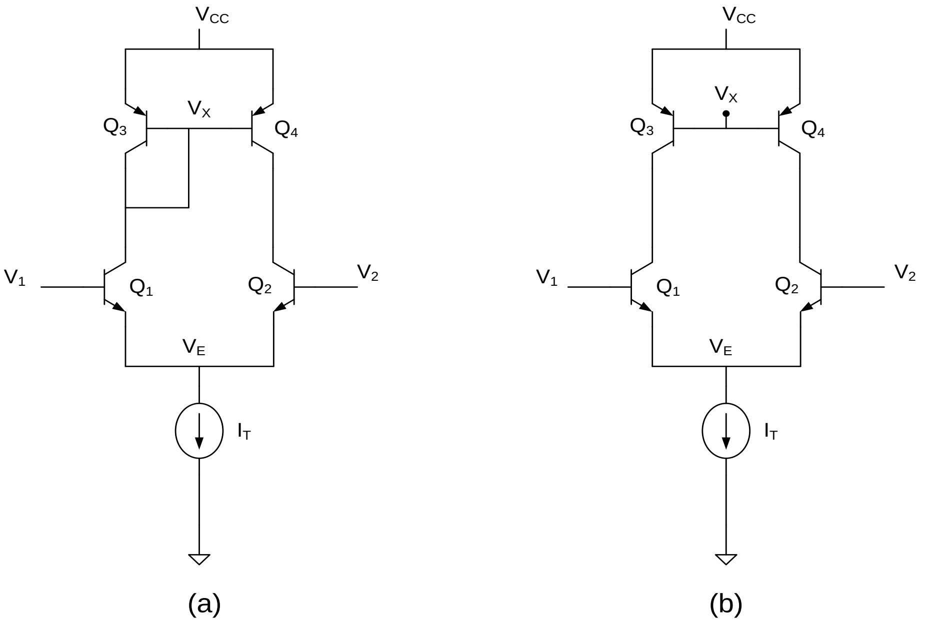
$$\sigma_{V_{OS}} \cong 7.2\text{mV}$$

$$3\sigma_{V_{OS}} \cong 21.6\text{mV}$$

Note this is much lower but still a large offset voltage !

The areas of M_1 and M_3 need to be very large to achieve a low offset voltage !!

Random Offset Voltages



It can be shown that

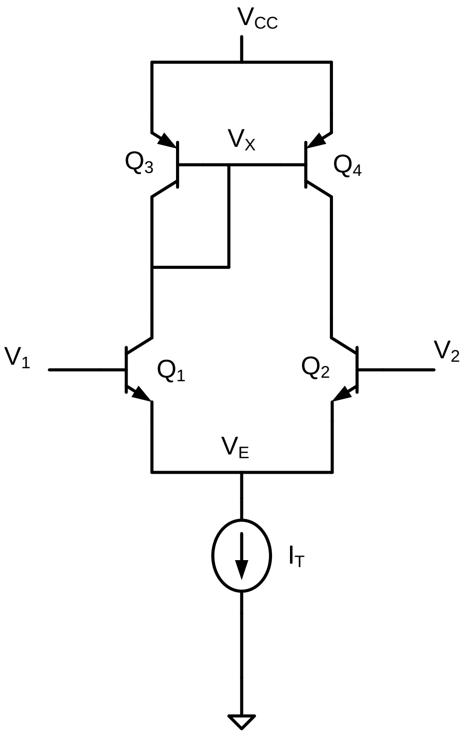
$$\sigma_{V_{OS}}^2 \cong 2V_t^2\left[\frac{A_{Jn}^2}{A_{En}}+\frac{A_{Jp}^2}{A_{Ep}}\right]$$

where very approximately

$$A_{Jn} = A_{Jp} = 0.1\mu$$

Random Offset Voltages

Example: Determine the 3σ value of the offset voltage of this bipolar input stage if $A_{E1}=A_{E3}=10\mu^2$



$$\sigma_{V_{OS}}^2 \cong 2V_t^2\left[\frac{A_{Jn}^2}{A_{En}}+\frac{A_{Jp}^2}{A_{Ep}}\right]$$

$$\sigma_{V_{OS}} \cong \sqrt{2}V_t\, A_J \frac{\sqrt{2}}{\sqrt{A_E}}$$

$$\sigma_{V_{OS}} \cong 2 \bullet 25\text{mV} \bullet 0.1\mu \bullet \frac{1}{\sqrt{10\mu^2}} = 1.6\text{mV}$$

$$3\sigma_{V_{OS}} \cong 4.7\text{mV}$$

Note this value is much smaller than that for the MOS input structure !

Random Offset Voltages

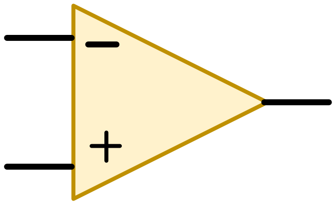
Typical offset voltages:

MOS - 5mV to 50MV
BJT - 0.5mV to 5mV

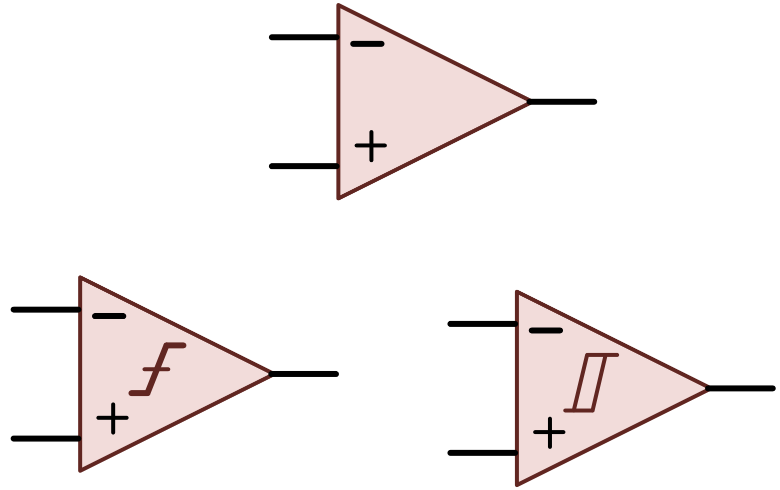
These can be scaled with extreme device dimensions

Often more practical to include offset-compensation circuitry

Offset Voltage in Comparators



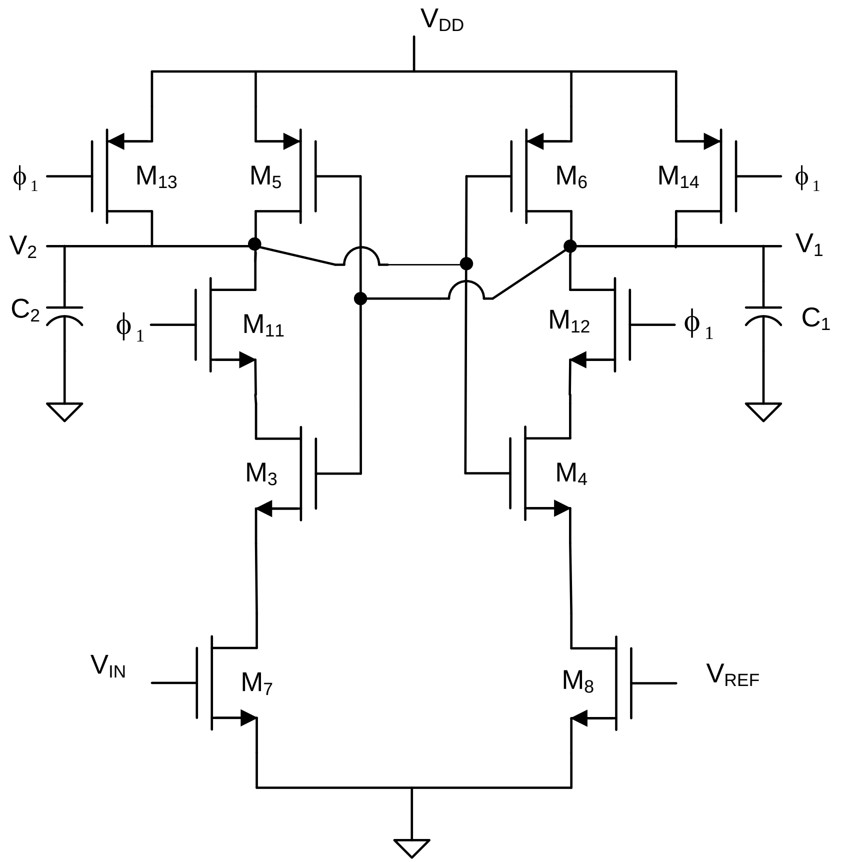
Op Amp



Comparator

- Op Amps Can be used as Comparators
- Comparators often have hysteresis in transfer characteristics
- Offset voltage of Comparators often key parameter in data converters

Offset voltage difficult to determine in come classes of comparators



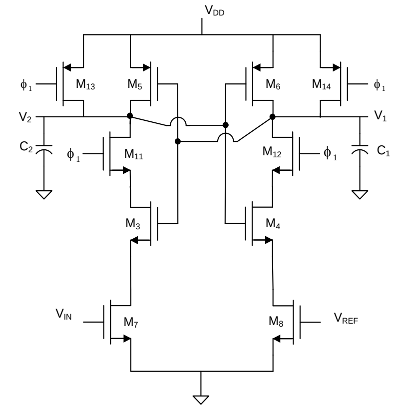
Dynamic clocked comparator

When φ_1 is low, V_1 and V_2 are precharged to V_{DD} and no static power is dissipated
When φ_1 is high, enters evaluate state and no static power is dissipated

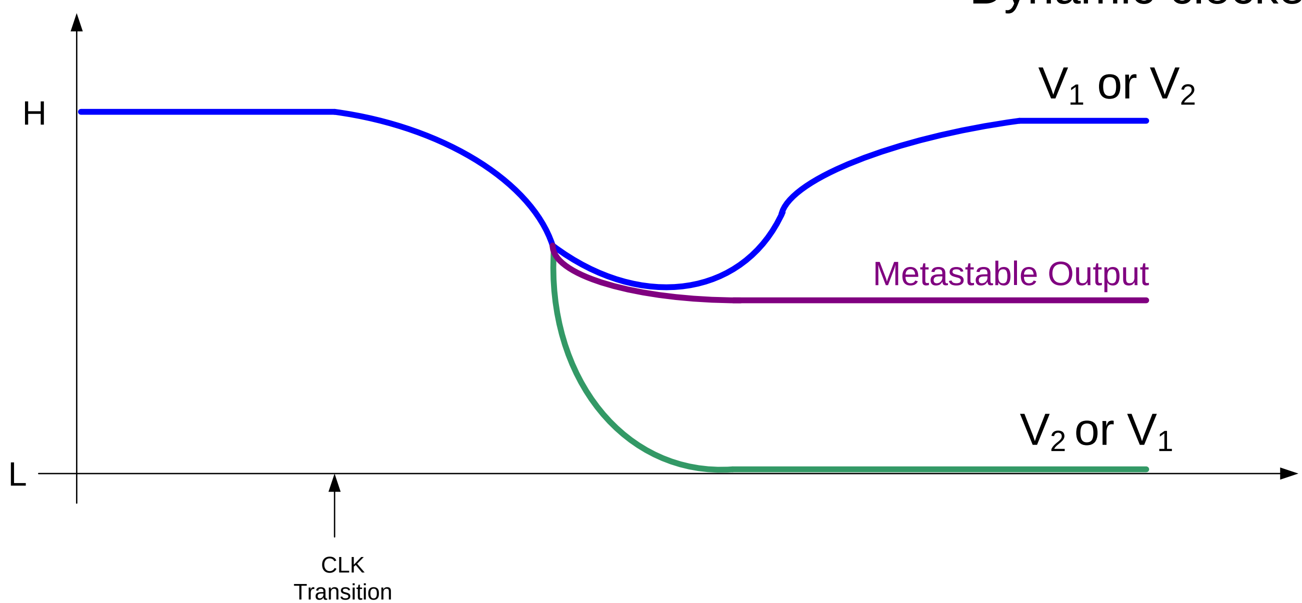
Offset voltage difficult to determine in come classes of comparators

Very small, very fast, low power

But offset voltage can be large (100mV or more)

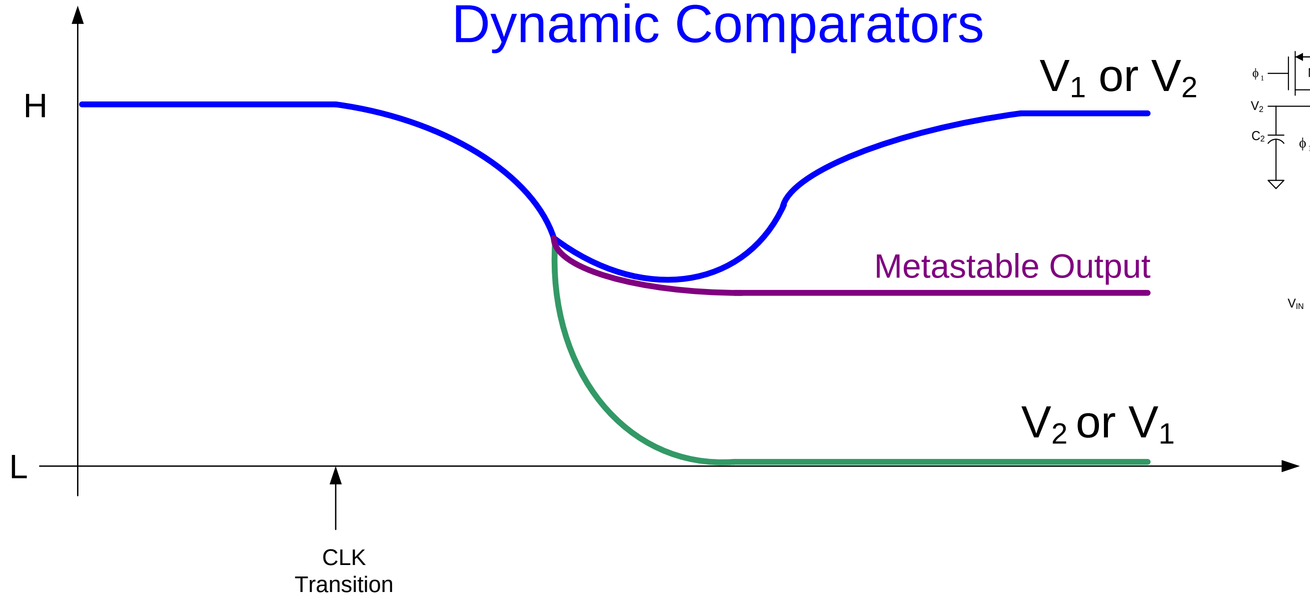


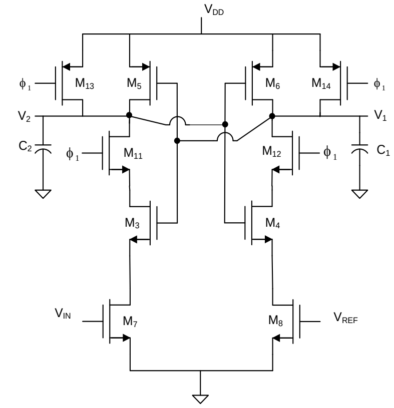
Dynamic clocked comparator



Decision is being made shortly after clock transition when devices are deep in weak inversion and signal levels are very small

Dynamic Comparators





Dynamic Comparators widely used because of low power dissipation

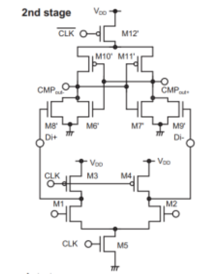
Often include one or more pre-amp stages before regeneration applied

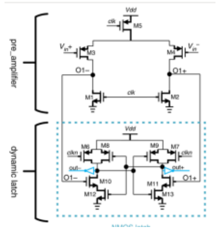
Previous-code dependence and kickback both of concern in dynamic comparators

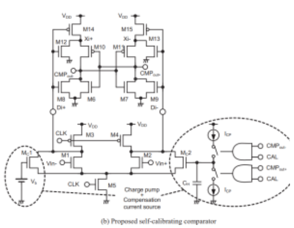
Noise may significantly affect performance and difficult to analyze and simulate because transient noise models in deep weak inversion are questionable

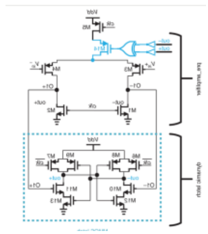
Still major opportunities to make significant improvement in dynamic comparators

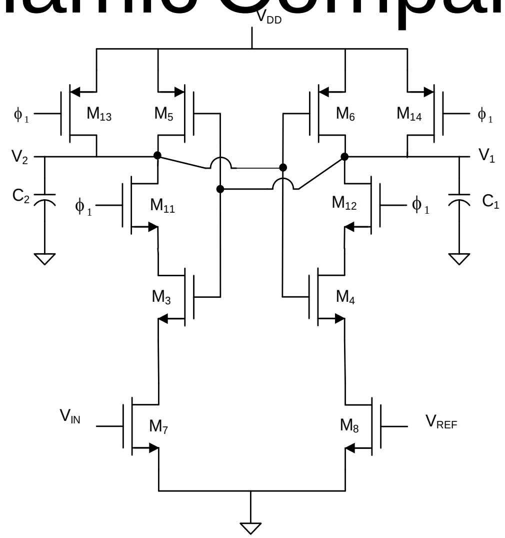
Dynamic Comparators

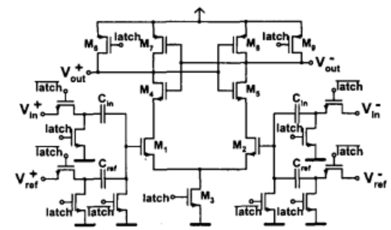


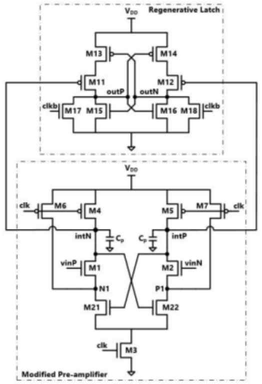












Relatively small number of dynamic comparators have been introduced

Significant difference in performance among those available

Analysis and performance assessment either analytically or via simulation not trivial

Opportunity to make significant advances in dynamic comparator design likely available

Analyses of static and dynamic random offset voltages in dynamic comparators
J **He**, S Zhan, D Chen, RL **Geiger** - IEEE Transactions on …, 2009 - ieeexplore.ieee.org
… **Geiger**, "Yield enhancement with optimal area allocation for ratio critical analog circuits," …
He, S. Zhan, D. Chen, and RL **Geiger**, "A simple and accurate method to predict offset voltage in …
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Additional details about offset voltage, statistical circuit analysis, and matching can be found in the draft document

“Statistical Characterization of Circuit Functions” by R.L. Geiger

Summary of Offset Voltage Issues

- Random offset voltage is generally dominant and due to mismatch in device and model parameters
- MOS Devices have large V_{OS} if area is small
- σ decreases approximately with $1/\sqrt{A}$
- Multiple fingers for MOS devices offer benefits for common centroid layouts but too many fingers will ultimately degrade offset because perimeter/area ration will increase (A_W and A_L will become of concern)
- Offset voltage of dynamic comparators is often large and analysis not straightforward
- Offset compensation often used when low offsets important

MOS: $$\sigma_{V_{OS}}^2 \cong 2\left[\frac{A_{VTOn}^2}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A_{VTOp}^2\right]$$

Bipolar: $$\sigma_{V_{OS}}^2 \cong 2V_t^2\left[\frac{A_{Jn}^2}{A_{En}} + \frac{A_{Jp}^2}{A_{Ep}}\right]$$

Stay Safe and Stay Healthy !

End of Lecture 11